A study on the low voltage operation of pentacene-based organic floating-gate memory utilizing N-doped LaB_6/LaB_xN_y stacked layer

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1. Introduction

The nitrogen-doped (N-doped) LaB_6 has low resistivity, low work function, and chemical stability [1]. Previously, we have reported the N-doped LaB_6 metal and LaB_xN_y insulator formation by Ar- and Ar/N_2-plasma sputtering for floating-gate memory applications [2,3].

In this study, the pentacene-based organic floating-gate memory with N-doped LaB_6/LaB_xN_y stacked layer was investigated.

2. Experimental procedure

The chemically cleaned n^+-Si(100) substrate was prepared for the control gate (CG). Next, the N-doped LaB_6 floating-gate (FG) and LaB_xN_y tunnel (TL) and block layer (BL) with a thickness of 5/20/10 nm, respectively, were in-situ formed by RF sputtering at room temperature (RT) using N-doped LaB_6 target (N: 0.4 %). In the case of the LaB_xN_y layer, the Ar/N_2-plasma sputtering was carried out with Ar/N_2 gas flow ratio of 10/7 sccm. The N-doped LaB_6 layer was formed by Ar-plasma sputtering with Ar gas flow rate of 10 sccm. Next, the post metallization annealing (PMA) process was carried out at 400°C/1 min in N_2 (1 SLM). Then, a 10 nm-thick pentacene channel layer was formed by thermal evaporation. Next, the Au top electrode (ϕ: 100 μm) was formed by the thermal evaporation method. The electrical characteristics of the fabricated organic floating-gate type diode were evaluated by C-V and program/erase (P/E) measurement at RT.

3. Results and Discussion

The C-V and P/E characteristics for pentacene-based organic floating-gate type diodes were shown in Fig. 1. The negligible hysteresis of 46 mV was obtained as shown in Fig. 1(a). This result suggested the excellent interface property between the pentacene and N-doped LaB_6 IL. The memory window (MW) of 1 V was obtained with program voltage and time (V_{PGM}/t_{PGM}) of -4 V/10 ms and the erase voltage and time (V_{ERS}/t_{ERS}) of 4 V/10 ms, although the hysteresis was increased from 38 mV to 77 mV as shown in Fig. 1 (b).

4. Conclusions

We investigated the pentacene-based floating-gate type diode utilizing N-doped LaB_6/LaB_xN_y stacked layer. The MW of 1 V was obtained with low V_{PGM} and V_{ERS} of ±4 V, and a pulse width of 10 ms. It would be promising for flexible organic floating-gate memory applications with low operation voltage.

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References

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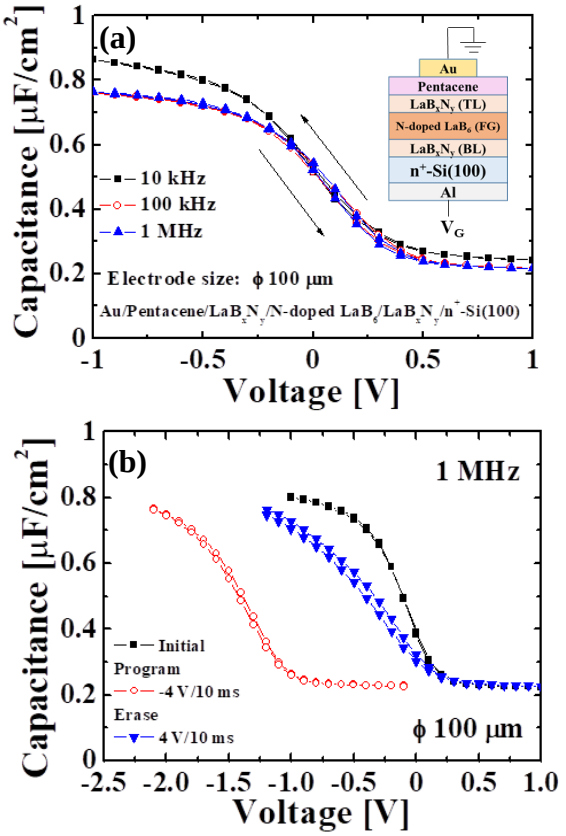

Figure 1. (a) C-V characteristics and (b) P/E characteristics of pentacene-based floating-gate type diode.