Impact of gate input pulse width on FeFET-based reservoir computing

○ Z. Wang, K. Toprasertpong, Z. Lin, E. Nako, R. Nakane, M. Takenaka and S. Takagi
The University of Tokyo, Faculty of Engineering
E-mail: wangzy@mosfet.t.u-tokyo.ac.jp

1. Introduction We have proposed a new physical system utilizing FeFETs [1] for reservoir computing (RC) [2]. FeFET-based RC is achieved by inputting triangle pulses on the gate terminal and treating the time-series drain current (I_d) as virtual nodes, shown in Fig. 1 [1]. Here, understanding physical mechanisms of RC using FeFETs is important for further improving their RC capacity. In this study, the relation between the gate pulse width and RC capacity is examined, and the origin of the pulse width dependence is explained.

2. Experiment A Si FeFET with a TiN/$Hf_{0.5}Zr_{0.5}O_2$(10 nm)/SiO_2 (0.7 nm) gate stack is used in this work. $Hf_{0.5}Zr_{0.5}O_2$ was deposited by ALD and annealed at 400 ℃ for 30 s. A FeFET with gate length of 10 μm and gate width of 100 μm is used for the experiments. Positive and negative triangle pulses, encoded as '1' and '0', respectively, are input as gate voltage. The pulses have swing of 3 V under the center voltage of 1 V and the pulse width is ranged from 2 μs to 0.1 s. During one pulse, I_d is equally sampled by 200 points, which are utilized as virtual nodes for training and testing. 1000 time-series random pulses with a given pulse width are used as input signals and a 10-fold cross-validation is applied. Short-term memory (STM) and parity check (PC) tasks are performed to examine the RC capacity [3].

3. Results and Discussion Fig. 2 shows the STM and PC capacity (C_{STM}, C_{PC}) as a function of the pulse widths. It can be found that higher RC capacity is achieved under pulses with shorter width. To understand the reason behind, correlations between predicted and correct values are shown in Fig. 3 as a function of the time step (T_{delay}). It can be found that the correlation at $T_{delay} = 2$ is decisive for total capacity, which is the accumulation of square of correlations over all T_{delay}. Therefore, analyzing the behavior at $T_{delay} = 2$ is crucial for understanding the physical origin of the pulse width dependence.

In STM and PC tasks judging from the present I_d waveform, it is necessary to separately discuss behaviors of I_d under positive and negative pulse at the present time. Thus, classification accuracy for positive or negative pulse is employed as the capacity evaluation, instead of correlation. The classification accuracy for $T_{delay} = 2$ is shown in Fig. 4 as a function of the pulse width. It can be found that accuracy for positive pulses, almost between 1 and 0.95, is much higher than that for negative ones. This fact indicates that C_{STM} and C_{PC} are mainly determined by the low accuracy under negative pulses. The blue lines in Fig. 4 show total C_{STM} and C_{PC}, which is in accordance with the accuracy under negative pulses.

The time response of I_d during the present pulse is shown in Fig. 5(a)-(d) to analyze the physical reasons. The legend refers to the input sequence, where the last number represents the current input pulse. For example, '110' in Fig. 5(b) represents the input signal of positive → positive → negative pulses in sequence. Here, in order to obtain the capacity of STM and PC tasks for $T_{delay} = 2$, the I_d waveform under '010' should be distinguished from that under '110'. Fig. 5(a) and (b) show the results with the pulse width of 0.02 s. I_d is not observed during most of the period, because the applied voltage is lower than the threshold voltage of the FeFET during this period. On the other hand, when pulse width is short enough (Fig. 5(c) and (d) with the pulse period of 2 μs), the distinguishable component of I_d is observed. This current component is attributed to charging/discharging current with changing gate voltage, which can be generated in the overlap region between the gate electrode and the drain region. As a result, it can be concluded that, when pulse width is short, extra information due to charging/discharging current under negative pulses is provided to distinguish the difference in the previous pulses in comparison with long pulse width, which eventually improves the STM and PC capacity.

4. Conclusions We have shown that input signals with shorter pulse width exhibit better RC capacity than those with longer one. This RC capacity improvement is attributed to charging/discharging current observed under fast-changing pulses, which provides extra information during negative pulses.

Acknowledgement This work was supported by JST CREST Grant Number JPMJCR20C3, Japan.

References [1] E. Nako, et al., *VLSI Symp.*, TN1.6 (2020). [2] H. Jaeger, *GMD Report* 148 (2001). [3] T. Furuta et al., *Phys. Rev. Applied* 10, 034063 (2018).

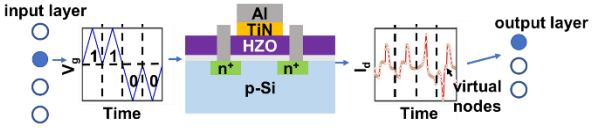

Fig. 1 Schematic of FeFET-based reservoir computing.

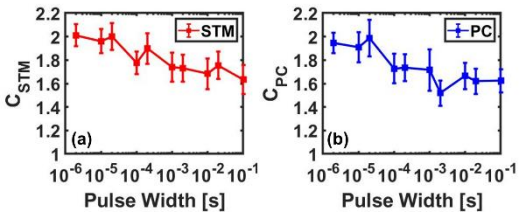

Fig. 2 Relation between capacity and pulse width for (a) STM (b) PC task.

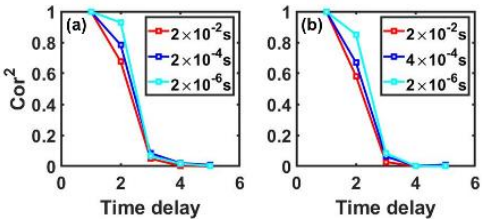

Fig. 3 Correlation with T_{delay} for (a) STM (b) PC task.

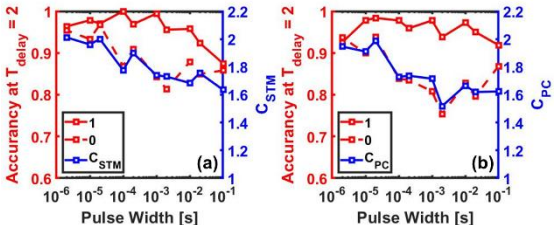

Fig. 4 Accuracy for $T_{delay} = 2$ with pulse width for (a) STM (b) PC task.

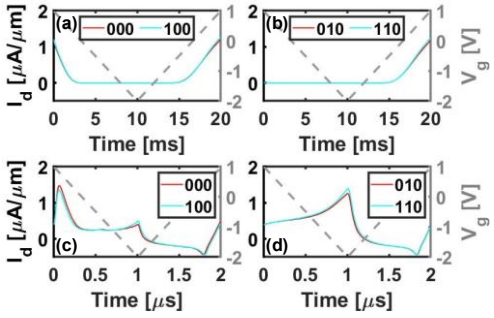

Fig. 5 V_g-t plot and I_d-t plot. (a)(b) Pulse width is 0.02 s. (c)(d) Pulse width is 2 μs.