Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp11-12

Critical Impact of Ferroelectric-Phase Formation Annealing on MFIS Interface of HfO_2-Based Si FeFETs

Kasidit Toprasertpong, Kento Tahara, Taichiro Fukui, Zaoyang Lin, Kouhei Watanabe, Mitsuru Takenaka, and Shinichi Takagi
The University of Tokyo, 7-3-1, Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone: +81-3-5841-6733, E-mail: toprasertpong@mosfet.t.u-tokyo.ac.jp

Abstract

We systematically study the impact of ferroelectric-phase formation annealing process on the MFIS interface of HfO_2-based Si FeFETs. While high-temperature annealing is favorable for activating the ferroelectricity, it forms an unintentional interfacial layer and significantly degrades the MFIS interface properties, resulting in degraded OFF current, memory window, *S.S.* value of FeFETs. As a solution to this temperature tradeoff, low annealing temperature of 400°C or lower is suggested for activating ferroelectricity in ALD-$Hf_{0.5}Zr_{0.5}O_2$/Si FeFETs while assuring the satisfactory interface quality.

1. Introduction

Ferroelectric doped HfO_2 as well as $Hf_xZr_{1-x}O_2$ compounds are highly CMOS-compatible and promising as a gate insulator in ferroelectric-gate field-effect transistors (FeFETs) [1]. It is generally known that thermal annealing is necessary to stabilize the non-centrosymmetric orthorhombic phase, activating the ferroelectricity in such materials. Even though there are a large number of researches investigating the optimal annealing process for maximizing the ferroelectricity [2,3], there is a lack of understanding of the appropriate annealing process when the ferroelectric layer is stacked on the semiconductor substrate as a FeFET gate insulator. As a result, the optimization of the annealing process becomes complicated as it will also affect the MFIS interface (MOS interface) properties of FeFETs [4]. In this work, we systematically investigate the impact of the ferroelectric-phase formation annealing process on the TiN/ALD-$Hf_{0.5}Zr_{0.5}O_2$/IL/Si MFIS interface (IL: interfacial layer) as well as the FeFET characteristics by studying a wide range of annealing temperatures, and discuss the process guideline for improving the performance of FeFETs.

2. Sample Preparations

We prepared ferroelectric devices with four configurations: MFM, MFIS$^+$ (highly-doped substrate), MFIS capacitors (10^{15}-cm^{-3} substrate), and FeFETs. The process flow is summarized in Fig. 1. Most processes, except device-specific processes in Fig. 1, were carried out simultaneously in a same chamber. After depositing $Hr_{0.5}Zr_{0.5}O_2$ by ALD and TiN by sputtering, samples were annealed at 300, 400, 500, 600, and 700°C for 30 s in N_2 atmosphere. The samples without annealing process were also prepared for reference. The TEM images of MFIS capacitors annealed at 400°C and 600°C in Fig. 2 indicate that the $Hr_{0.5}Zr_{0.5}O_2$ layer is 10-nm thick and confirms that there is no change of the $Hr_{0.5}Zr_{0.5}O_2$ thickness for different annealing conditions. The gate-last process was employed for fabricating FeFETs in order to avoid the influence of S/D activation annealing when we investigate the impact of ferroelectric-phase formation annealing.

2. Experimental Results

Fig. 3 shows the *P*-*V* characteristics of MFM, MFIS$^+$, and MFIS capacitors. As can be expected, the amount of switching polarization P_{SW} ($=P_{r+}-P_{r-}$, Fig. 4) in the MFM capacitors is improved with increasing annealing temperature until 700°C. No ferroelectricity is observed when the annealing temperature is below 300°C, implying that the ferroelectric phase in our ALD-$Hf_{0.5}Zr_{0.5}O_2$ starts to crystallize from around 400°C. On the other hand, the MFIS$^+$ capacitors exhibit the opposite behavior, showing decreased P_{SW} at high annealing temperature. This behavior is attributed to the unintentional formation of IL at the $Hf_{0.5}Zr_{0.5}O_2$/Si interface after high temperature annealing as observed in the TEM images in Fig. 2. Since IL has much lower dielectric constant (~3.9) than $Hf_{0.5}Zr_{0.5}O_2$ (~30), the formation of only thin IL can cause a large voltage drop and reduces the voltage across $Hf_{0.5}Zr_{0.5}O_2$, hindering the polarization reversal. It is interesting to note that ferroelectricity cannot be observed from *P*-*V* measurements on the MFIS capacitors having low-doped substrates (Fig. 3(c)) due to the artifact from deep depletion in Si substrates during *P*-*V* measurements with fast voltage scan [5].

Fig. 5 shows the *C*-*V* characteristics of the MFIS capacitors. The scanning voltage was chosen to be relatively small, ±2 V, to minimize the effect of polarization-induced charge trapping [6] in the *C*-*V* analysis. The EOT shown in Fig. 6, estimated from the accumulated capacitance, decreases after annealed at 400°C due to the formation of high-*k* ferroelectric phase, and increases monotonically at elevated temperature over 400°C due to the IL formation. Fig. 7 shows the interface state density D_{it} estimated from the High-low method using the capacitances at 1 MHz and 1 kHz. It clearly shows that, although the low-temperature annealing helps decrease D_{it} existing at the interface with as-deposited films, annealing temperature over 500°C notably increases D_{it}. This can be observed in the degraded steepness of the capacitance modulation in the *C*-*V* characteristics of the MFIS capacitors annealed at high temperature. The similar tendency of D_{it} and IL thickness implies that the increase of D_{it} could be related to the formation of unintentional IL.

Fig. 8 shows the I_d-V_g characteristics of FeFETs. As-deposited and 300°C-annealed FETs exhibit electron-trap hysteresis, consistent with the results of non-ferroelectricity from *P*-*V* measurements. FETs annealed at temperature from 400°C exhibit the operation as FeFETs confirmed by ferroelectric hysteresis. The memory window (MW) is summarized in Fig. 9. Annealing at low temperature of 400°C provides MW higher than 2.0 V with 10-nm-thick $Hf_{0.5}Zr_{0.5}O_2$. Except for the 500°C FeFET whose MW slightly increases owing to thicker EOT, high-temperature annealing generally degrades the memory window because of lower P_{SW} (Fig. 3(b)) as well as larger electron-trap hysteresis, caused by the poor interface, superimposed in MW [7]. Fig. 10 summarizes the *S.S.* values for forward and backward scans, showing that the poor MFIS interface in samples annealed at high temperature significantly degrades the subthreshold characteristics. The OFF current is also found to be high in samples without annealing and with high annealing temperature, which is in agreement with the tendency of D_{it}. This is attributable to the recombination current at the MFIS interface that is in contact with the *p*-*n* junction depletion region.

The above findings suggest that low temperature annealing is necessary to maintain the satisfactory MFIS interface quality. In other words, the optimal temperature would be close to the lower limit of crystallization temperature of the ferroelectric phase, which is 400°C in this study. Further lowering the crystallization temperature [8] would be an effective

approach to further improve the performance of FeFETs.

3. Conclusions

We systematically investigate the impact of the annealing process on the MFIS interface properties of FeFETs. We have found the notable tradeoff between the ferroelectricity and the MFIS interface properties at elevated annealing temperature. This suggests that FeFETs should be prepared at annealing temperature as low as possible but still sufficient to form the ferroelectric phase to achieve high-performance FeFETs.

Acknowledgements This work was supported by KIOXIA Corporation, JSPS KAKENHI Grant No. 17H06148 and 19K15021, and JST CREST Grant No. JPMJCR1332, Japan.

References

[1] J. Müller *et al*, IEEE Electron Device Lett. **33** (2012) 185.
[2] M. H. Park *et al*, Appl. Phys. Lett. **102** (2013) 242905.
[3] T. Mimura *et al*, Jpn. J. Appl. Phys **58** (2019) SBBB09.
[4] Y.-H. Chen *et al*, IEEE Electron Device Lett. **40** (2019) 467.
[5] K. Toprasertpong *et al*, Appl. Phys. Lett. **116** (2020) 242903.
[6] K. Toprasertpong *et al*, IEDM Tech. Dig. (2019) 570.
[7] K. Toprasertpong *et al*, Proc. VLSI Symp. (2020) TF1.5.
[8] T. Onaya *et al*, Microelectron. Eng. **215** (2019) 111013.

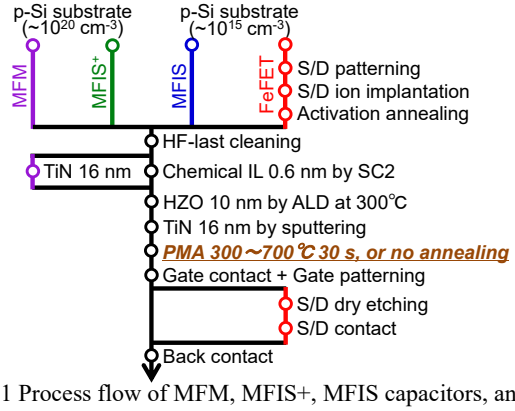

Fig. 1 Process flow of MFM, MFIS+, MFIS capacitors, and FeFET

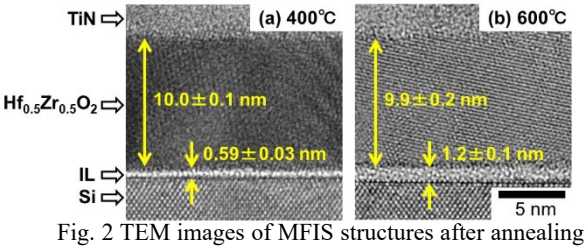

Fig. 2 TEM images of MFIS structures after annealing at (a) 400°C and (b) 600°C

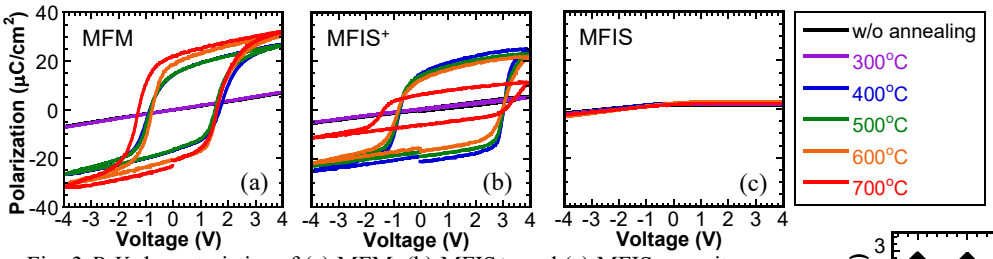

Fig. 3 *P-V* characteristics of (a) MFM, (b) MFIS+, and (c) MFIS capacitors annealed at different temperatures. The leakage compensation has been performed.

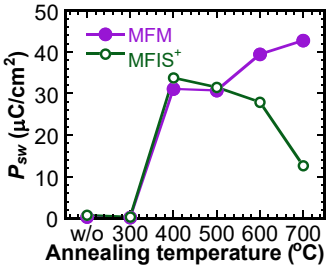

Fig. 4 Switching polarization of MFM and MFIS+ capacitors

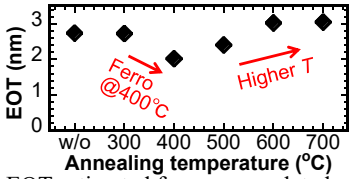

Fig. 6 EOT estimated from accumulated capacitance.

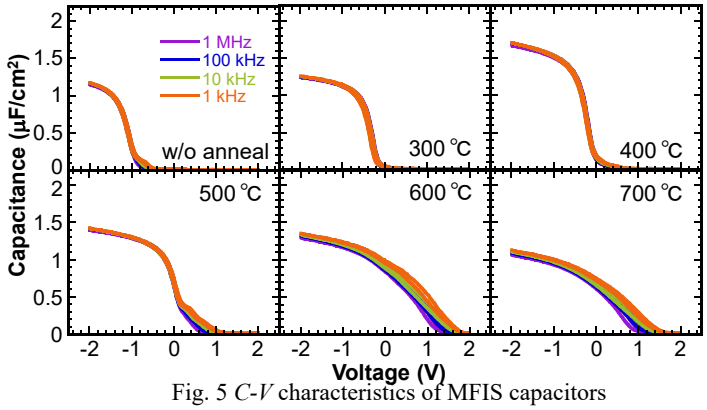

Fig. 5 *C-V* characteristics of MFIS capacitors

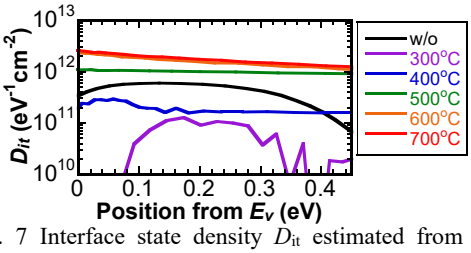

Fig. 7 Interface state density D_{it} estimated from the High-low method

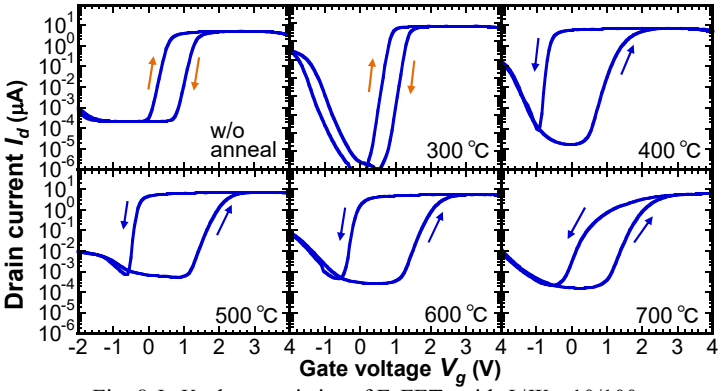

Fig. 8 I_d-V_g characteristics of FeFETs with L/W = 10/100 μm

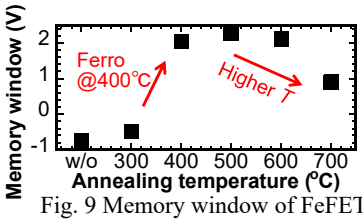

Fig. 9 Memory window of FeFETs

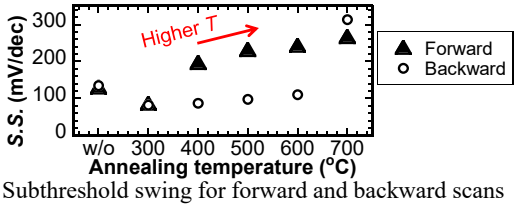

Fig. 10 Subthreshold swing for forward and backward scans