Materials and Layer Transfer Process Technologies for Heterogeneous 3D Integration of Germanium on Silicon (Invited)

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Abstract— This paper describes key heteroepitaxy and layer transfer process technologies that enable demonstration of monolithic heterogeneous 3D integration of germanium on 300mm silicon. A Ge PMOS transistor with the best-ever reported I_{ON}-I_{OFF} performance has been achieved using this layer transfer technology.

1. Introduction

Germanium transistors hold a great promise to extend Moore's Law scaling, specifically to fulfill the inescapable need for continuing power supply scaling while maintaining performance. Owing to its high carrier mobility, logic CMOS with germanium as the channel material may deliver the best drive current and energy vs. delay performance [1]. Unlike the long-established Si CMOS manufacturing technology, high volume fabrication of Ge transistors on bulk substrates would be very cost prohibitive. However, recent advances in layer transfer and monolithic heterogeneous 3D integration technologies have enabled a more practical and economical approach to integrate Ge with existing silicon technology platform [2-5].

This paper highlights advances in epitaxy and 3D layer transfer technologies that enable high-performance Ge PMOS on 300mm Si platform. Ge PMOS with excellent device characteristics and record I_{ON} = 497 μA/μm at I_{OFF} = 8 nA/μm and V_{DS}= -0.5V have been demonstrated. It represents the best I_{ON}-I_{OFF} performance achieved with Ge channel PMOS transistor reported to date [2].

2. 300mm Ge Heteroepitaxy and Layer Transfer Process

The layer transfer process flow to achieve monolithic 3D stacking for Ge transistors on Si transistors is depicted in Fig.1. A single-crystal Ge (100) film is epitaxially grown via a buffer layer designed to mitigate Ge and Si lattice mismatch defects. Optimization of this buffer layer is key to obtaining high quality donor epi for the layer transfer. A Ge film with Hall mobility as high as 1600 cm2/V.s at ns= 7e16/cm3 has been achieved (Fig. 2a). The Ge donor epi wafer is subsequently implanted with a high dose of H+ implant to create a fracture sub-layer in the Ge film. The wafer is flipped and bonded to the Si NMOS device wafer. The donor wafer is then cleaved away through a series of anneal steps, leaving a high-quality thin layer of Ge on the device wafer. Hall mobility of Ge measured after the layer transfer still closely matched to the donor value, confirming no degradation with Ge after the layer transfer (Fig. 2b).

Several polish and clean steps are then employed to produce a clean and smooth Ge layer on the device wafer. Fig. 3 shows layer transfer Ge thickness contour map on the 300mm wafer measured with spectroscopic ellipsometry. Ultrathin body Ge with thickness variation <1.5nm across 300mm wafer has been demonstrated.

3. Low temperature processes for sequential 3D stacking

Sequential 3D stacking of Ge with Si is very attractive because of the low process thermal budget associated with layer transfer and Ge device fabrication. Keeping the maximum process temperature at 600 °C together with some optimization on Si metal gate stack have been shown to maintain device characteristics of the bottom Si transistors. Fig. 4 shows matched transfer characteristics, including $I_{D,SAT}$, $I_{D,LIN}$, V_T, and subthreshold slope (SS) of Si FinFET NMOS before and after stacking. There is no change in gate stack and external resistance (R_{EXT}), evidenced by the absence of Vt shift and drive current degradation on Si NMOS post 3D stacking.

4. Layer Transfer Ge PMOS Device Characteristics

High quality, ultra-thin gate dielectric oxide is necessary for high performance Ge PMOS transistor. Novel surface preparation technique comprising of dry clean and surface passivation processes were implemented in combination with high pressure anneal (HPA) to achieve oxide interface with low defect density Dit < 4E11 $eV^{-1}cm^{-2}$ (Fig. 5). High quality Ge channel sourced from the layer transfer in concert with this low Dit gate dielectric interface have produced Ge PMOS transistors with outstanding characteristics. A high mobility of 225 $cm^2 V^{-1} s^{-1}$ at n_s=5e12 cm^{-2} and EOT = 5.7A, which is the highest mobility among Ge channel MOSFETs at ultra-thin EOT reported in the literature [6-12], was achieved (Fig. 6). Gate all-around (GAA) transistor architecture (Fig. 7) and well passivated gate oxide interface also contributed to excellent electrostatics. The device exhibits SS_{LIN} = 61 mV/dec, SS_{SAT} = 68 mV/dec, DIBL=14mV/V at Lg = 34nm and I_{ON} = 497 μA/μm at minimum I_{OFF}= 8 nA/μm and 0.5V V_G swing from OFF to ON (Fig. 8), which is a record I_{ON}-I_{OFF} performance surpassing the leading shortchannel Ge PMOS reported in the literature [7, 13-16] shown in Fig. 9. Ge devices in this study also maintain the high drive performance at the gate length relevant to leading edge technology nodes (Fig.10).

5. Conclusion

Heterogeneous 3D integration of Ge on Si has been made possible by advances in heteroepitaxy and layer transfer process technologies. High performance short channel Ge PMOS transistors with the record gain at V_{CC} = 0.5V have been experimentally demonstrated on a 300mm Si platform. The Ge transistors in this study demonstrate a viable option for low power high performance CMOS logic applications and for continuing Moore's law in future technology nodes.

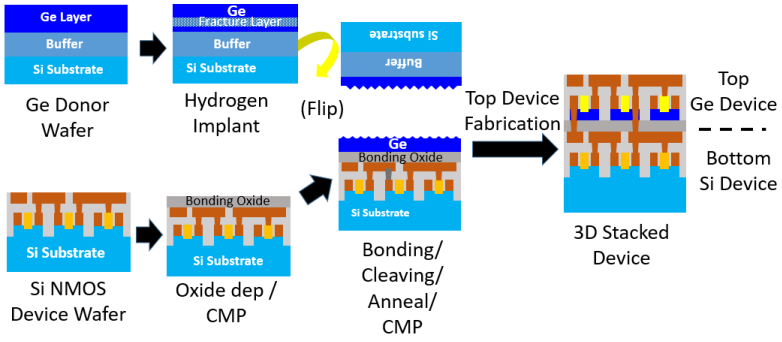

Fig. 1. Process flow for sequential 3D integration of Ge PMOS and Si NMOS. Ge is epitaxially grown on 300mm Si donor wafer via a buffer layer, which is then layer transferred onto a fully fabricated Si FinFET device wafer. Ge Gate-all-around (GAA) PMOS transistors are subsequently fabricated using the replacement metal gate (RMG) flow.

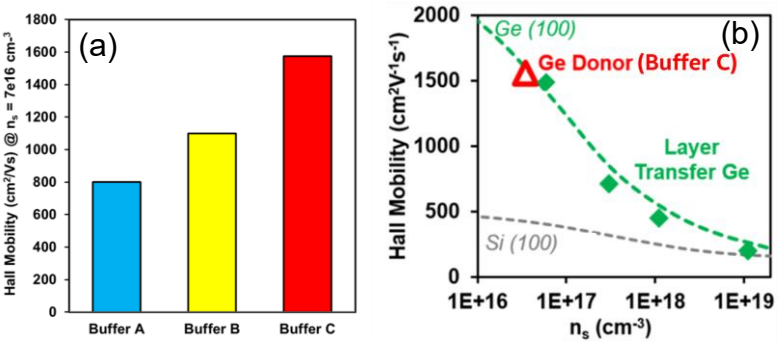

Fig. 2 Hall mobility vs hole density at 300K for (a) Ge Donor with different buffer epi recipes and (b) Ge layer transferred onto 300mm Si wafer. Ref [2]

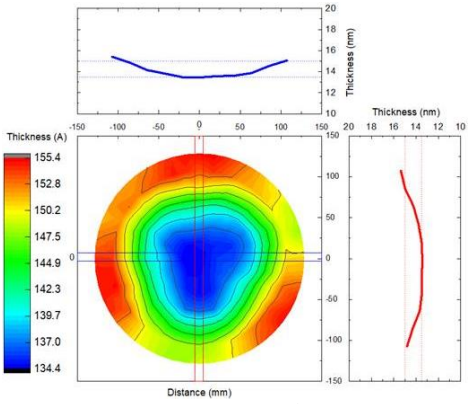

Fig. 3. Layer transfer Ge thickness contour map on 300mm wafer measured with spectroscopic ellipsometry with 15mm wafer edge exclusion.

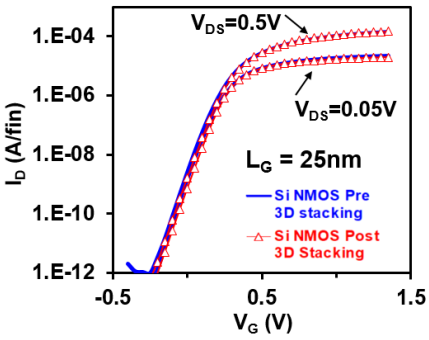

Fig. 4 I_D-V_G of Si FinFET NMOS single layer control (Pre 3D stacking) and bottom Si NMOS of the 3D stacked Ge-Si CMOS (Post 3D stacking). Ref [2]

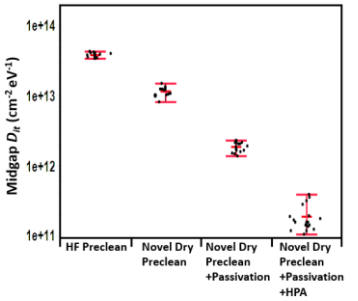

Fig. 5. Interface state density Dit (cm^{-2} eV^{-1}) as function surface treatments.

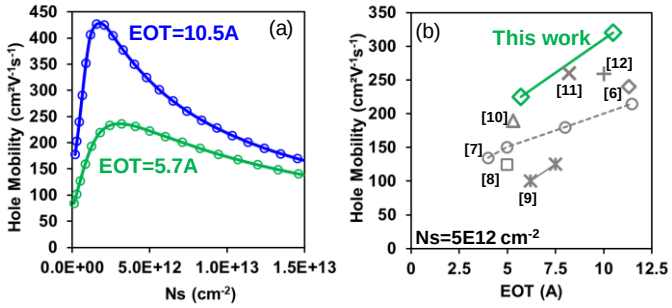

Fig. 6. (a) Mobility vs inversion charge density (n_s) on Ge GAA PMOS at two different gate oxide thicknesses, EOT = 5.7A and 10.5A, and (b) Mobility vs EOT benchmarked at n_s = 5e12 cm^{-2}. Ref [2]

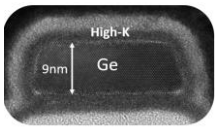

Fig. 7 Cross-sectional TEM of the gate all around (GAA) Ge nano-ribbon channel. Ref [2]

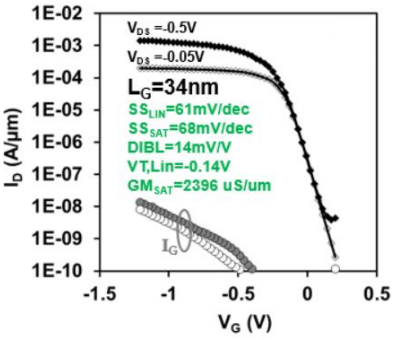

Fig. 8. I_D-V_G characteristics of shortchannel Ge GAA PMOS at V_{DS} = -0.05 and -0.5V and L_G = 34nm. Ref [2]

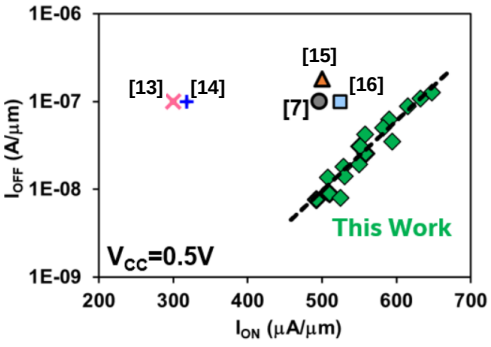

Fig. 9. I_{ON} vs I_{OFF} extracted at V_{DS} = -0.5V with the total V_G swing from I_{OFF} to I_{ON} of 0.5V. The Ge GAA PMOS exhibits record I_{ON}/I_{OFF} performance, surpassing all shortchannel Ge PMOS reported in the literature [3-7]. Ref [2]

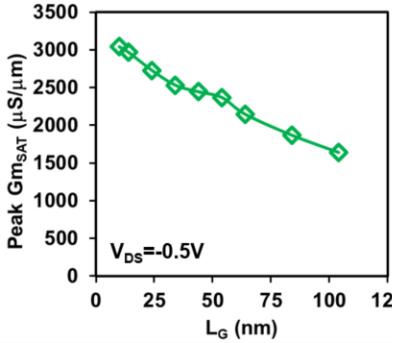

Fig. 10. Extrinsic peak Gm_{SAT} vs L_G of Ge GAA PMOS at V_{DS}=-0.5V. This demonstrates that the high transconductance has not saturated at scaled gate length below 25nm. Ref [2]

References

[1] R. Kim *et al.*, *IEDM Tech. Dig.*, 2015, pp. 875-878. [2] W. Rachmady *et al.*, *IEDM Tech. Dig.*, 2019, pp. 697-700. [3] H.W. Then *et al.*, *IEDM Tech. Dig.*, 2019, pp. 402-405. [4] M. Vinet *et al.*, *Proc. IEEE S3S Conf.*, 1 (2014). [5] G. Fitzgerald, *Proc. IEEE S3S Conf.*, 2b.1 (2017). [6] R. Pillarisetty *et al.*, *IEDM Tech. Dig.*, 150 (2010). [7] B. Duriez *et al.*, *IEDM Tech. Dig.*, 522 (2013). [8] M.J.H. van Dal *et al.*, *IEDM Tech. Dig.*, 492 (2018). [9] Y. Shin *et al.*, *VLSI Symp. Tech. Dig.*, 102 (2014). [10] S.H. Yi *et al.*, *EDL,* 38(5), 544 (2017). [11] R. Zhang *et al.*, *IEEE TED,* 60(3), 927 (2013). [12] R. Xie *et al.*, *IEDM Tech. Dig.*, 393 (2008). [13] L.Witters *et al.*, *IEEE TED,* 64 (11), 4587 (2017). [14] E. Capogreco *et al.*, *IEEE TED* 65 (11),5145 (2018). [15] H.Arimura *et al.*, *IEDM Tech. Dig.*, 496 (2018). [16] E. Capogreco *et al.*, *VLSI Tech. Symp.* 193 (2019).