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Implementation of Asymmetric Channel Implant in FDSOI Technology for Superior Analog Performance

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Abstract

In this work asymmetric implantation has been performed on FDSOI technology for improving analog performance. Different integrations schemes are presented. The possibility of g_m increase up to +65% is shown.

Introduction

Parallel to aggressive device scaling, technology differentiation is the new driver for major foundry players [1]. New markets require superior device performance not exclusively on standard logic cells, but also on RF/mmWave, analog, ultra-low voltage and ultra-low power devices. In particular, analog applications are getting momentum thanks to the high market request. The device transconductance (g_m) at in weak inversion and moderate field conditions is the major figure of merit for this market [2].

A powerful knob to improve g_m is the optimization of the source and drain junctions [3]. In particular, the use of asymmetric junction has been proven on bulk technologies to significantly increase the transistor transconductance [4-5].

In this work, we integrated the use of asymmetric pocket implant on 22FDX® technology. The device integration is presented in Section II. Section III discusses the electrical results and different possibility for asymmetric implantations.

Device Schematic

The devices considered in this work are fabricated using the 22nmFDX technology from GLOBALFOUNDRIES [6]. The process flow and the resulting device schematic of the device architecture are given in Figures 1 and 2. Silicon-on-Insulator (SOI) substrate wafers with a buried-oxide (BOX) thickness of ~ 20nm have been used. The silicon channel, featuring a final thickness of ~ 6nm, was kept un-doped. Raised source and drain are integrated to reduce contact to channel resistance. The asymmetric junction was obtained by performing an additional pocket implantation before the gate stack formation (highlighted step in Figure 1). Other than dose and implant energy, major fabrications knobs are pocket width (p_w) and relative distance to the source (x_s) (see Figure 2). Next section discusses how to optimize the asymmetric integration for maximum transconductance improvement.

In order to increase the measurement stability and data robustness, more than 60 instances with the same dimensions have been measured and the median value were reported each time. g_m has been measured for medium V_{DS} and V_{GS} conditions, regime most interesting for analog applications.

Transconductance boost by asymmetric implant

A. Implementation of asymmetric device

Figure 3 shows the measured g_m for different implant locations. The initial un-doped channel is compared to uniform channel implant. Clear g_m degradation is measured due to increased mobility channel scattering. Additionally, the transconductance measured on devices with asymmetric implant is reported. Here, the pocket implant has been locally applied or on the source side or on the drain side. Only when the channel implant is performed near to the source junction evident g_m improvement is measured (+12%). To explain the results, calibrated TCAD simulations of the electric field on the device junctions have been performed (Figure 4). For asymmetric device (red curve), two electric field peaks are present: one typical close to drain side and another one close to the source area. This peak is not present for un-doped transistors (black curve). For asymmetric case, this second electric field leads to higher field (i.e., steeper junction) and consequently to higher mobility.

B. Optimization of asymmetric implant for maximum g_m boost

Figure 5 reports the measured g_m for different pocket implant doses for short (plain symbols) and long (empty symbols) transistors. Maximum g_m is a function of implant dose as well used device channel length. Thus, it is important to setup the appropriate integration dose according to the used devices in the circuit application. Figure 6 shows the measured g_m dependency versus x_s and p_w for short (plain symbols) and long (empty symbols) devices. Evident g_m increase is obtained moving the implant pocket from the source side toward the middle of the channel. Additionally, maximum transconductance boost is measured for sharp and localized pocket implant (i.e., narrow p_w).

In conclusion, the intrinsic gain (g_m/I_D) versus drain current I_D are presented in Figure 7 for short (a) and long (b) channel devices. Standard un-doped transistors (blue curve) are compared to asymmetric devices (red curve) with pocket implant applied near to the source junction. Evident g_m/I_D improvement is obtained for both cases.

Conclusion

In this work we discussed the possibility to improve the analog performance of an FDSOI transistor by implementing asymmetric pre-gate implants. The optimum integration scheme must be aligned to the circuit requirements.

References

[1] G. L. Pattorn, ESSDERC, 2018 [2] C. Yi-P. Chao et al., IEEE J. EDS, 2016, [3] Y Taur, TH Ning - Cambridge, UK, 1998, [4] H. Shin et al., IEEE T-ED 1999, [5] S. Odanake et al., IEEE T-ED 1999 [6] R. Carter et al., IEDM 2016.

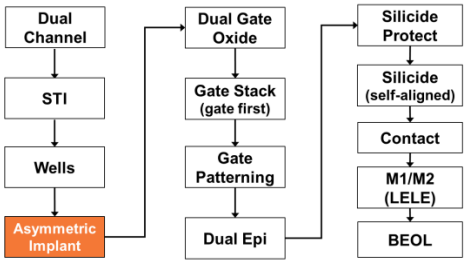

Figure 1: Standard 22nmFDX process flow. Asymmetric pocket implant was implemented before gate stack module

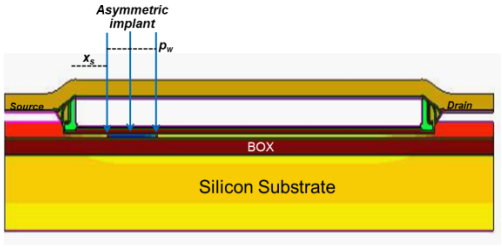

Figure 2: Simple schematic of asymmetric channel implant implemented in 22nmFDX silicon film. The distance between the source and the pocket implant is labeled x_s while the corresponding pocket width is p_s

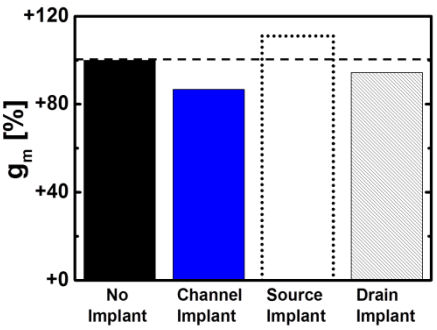

Figure 3: g_m measured on devices with different channel implant. +12% g_m boost with asymmetric source pocket implant

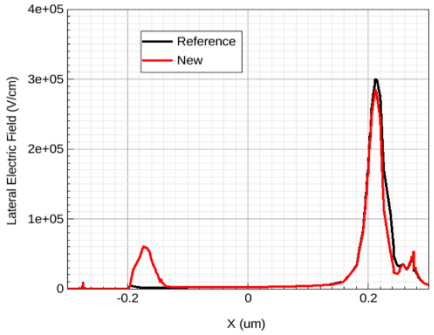

Figure 4: Lateral electric field for no-implanted (black) and implanted (red) devices. Evident field peak near the source region for asymmetric implanted device

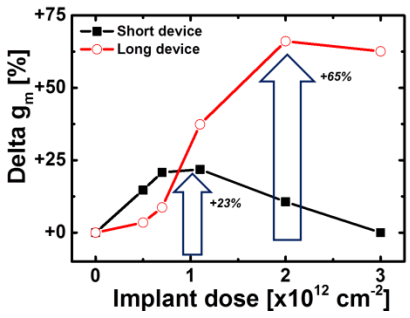

Figure 5: Relative g_m to no implant condition versus implant dose for short and long channel device. According to the device length. appropriate implant dose must be implemented to achieved maximum g_m boost

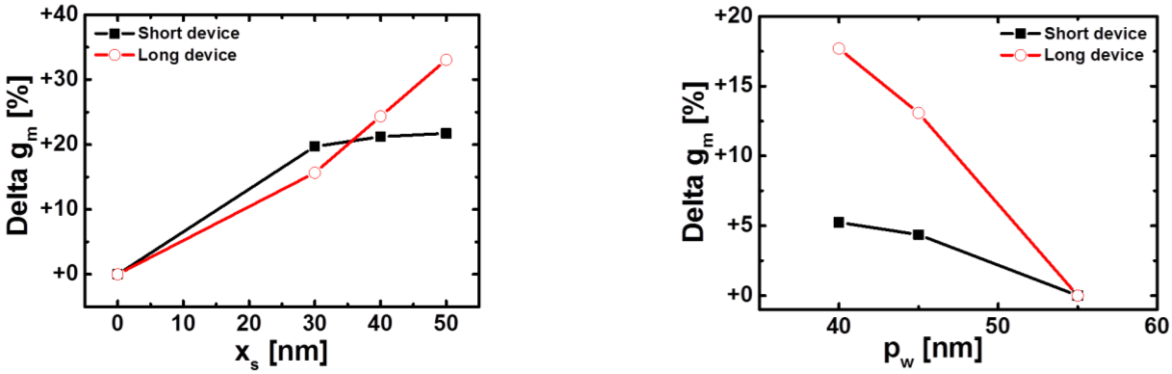

Figure 6: Measured g_m (normalized to the no implant condition) versus implant distance from the source x_s (a) and pocket width is p_s (b) for short (plain symbols) and long (empty symbols) devices. g_m increases for higher x_s, while a localized asymmetric implant is preferable for transconductance boost

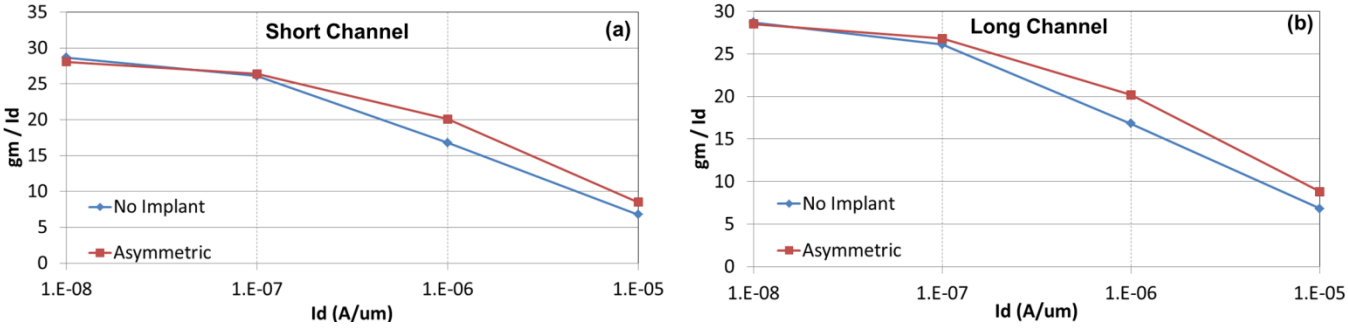

Figure 7: Intrinsic gain versus drain current for short (a) and long (b) gate length. A standard transistor without implant (blue curve) is compared to devices with asymmetric source implant (red curve). Evident intrinsic gain boost is obtained with asymmetric implant