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New Observation and Mechanism of Flicker Noise and Random Telegraph Noise in Sub-40nm SiC Strained nMOSFETs

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Abstract

The Silicon-Carbon (SiC) strained nMOSFETs can realize significant enhancement of the effective mobility (μ_{eff}) and drain current (I_{DS}) but reveal peculiar penalties in the flicker noise and random telegraph noise (RTN). The measured RTN features a complex spectrum with multi-level drain current fluctuation amplitudes and abnormally long capture and emission time constants (τ_c and τ_e). The new observation indicates severe deviation from the widely used elastic tunneling model by McWhorter and suggests new mechanisms like electron-phonon coupling responsible for the anomalously slow trapping/detrapping properties in the SiC strained nMOSFETs with ultra-thin gate oxide.

I. Introduction

Uniaxial strain has been proven a successful solution for mobility enhancement in nanoscale CMOS devices [1]-[2]. In this paper, SiC strained nMOSFETs were fabricated in 40 nm CMOS technology as a high mobility device platform aimed at high speed and high frequency applications [3]-[4]. However, the potential impact on flicker noise from the SiC strain appears as a critical concern for RF and analog circuits design, particularly for the CMOS oscillators vulnerable to close-in $1/f^3$ phase noise due to flicker noise up-conversion [5]. Moreover, the anomalous RTN spectrum with multi-level noise amplitudes emerging from SiC strained nMOS may cause worse jitter noise and bit error rate in high speed oscillators, but the underlying mechanism remains an open question and becomes a serious topic worthy of extensive research effort.

II. Mobility enhancement of SiC strained nMOSFET

Fig. 1(a) indicates that nMOSFETs require tensile stress at both longitudinal and transverse directions, namely $\sigma_{//}$ and $\sigma_{\perp}$ for electron mobility enhancement. In this paper, SiC strained nMOSFETs were fabricated by carbon implantation and regrowth by solid phase epitaxy, i.e. SiC SPE in source/drain extension (SDE) region, as shown in Fig. 1(b). A comparison of the channel current, I_{DS} vs. V_{GT} measured from SiC strained and control nMOSFETs shown in Fig. 2(a) indicates 23% increase of I_{DS} in SiC strained nMOS, which suggests mobility enhancement from the tensile $\sigma_{//}$. Herein, the effective mobility μ_{eff} can be extracted from the I_{DS} vs. V_{GT} characteristics, according to the linear I-V model given by (1)~(2) with W=10μm and L=32.85nm/35.05nm **[6]**. As shown in Fig.2(b), the SiC strained nMOS can successfully realize 20~27% higher μ_{eff} through V_{GT} and 22.5% enhancement of the peak μ_{eff}, compared to the control nMOS,

$$I_{DS} = \frac{W}{L} C_{ox(inv)} \mu_{eff} \left(V_{GS} - V_T - \eta V_{DS}\right) V_{DS} \quad (1)$$

$$\mu_{eff} = \frac{L}{WC_{ox(inv)}} \cdot \frac{I_{DS}}{\left(V_{GS} - V_T - \eta V_{DS}\right) V_{DS}}, \; 0 < \eta \le \frac{1}{2} \quad (2)$$

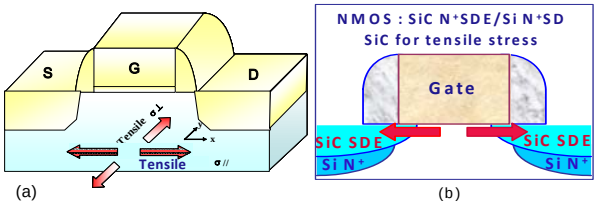

Fig. 1 (a) Uniaxial stress $\sigma_{//}$ and $\sigma_{\perp}$ favorable for mobility enhancement in nMOS (b) SiC strained nMOS with tensile $\sigma_{//}$ created by SiC SPE in SDE

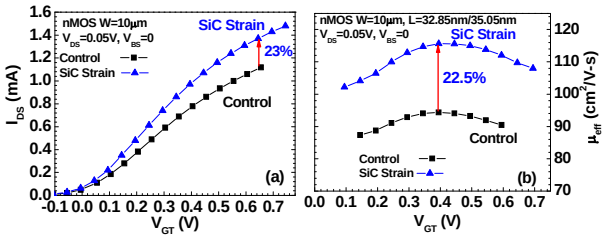

Fig.2 Comparison of SiC strained and control nMOSFETs with W=10μm, L=32.85nm/35.05nm (a) I_{DS} vs. V_{GT} (b) μ_{eff} vs. V_{GT} , V_{DS}=0.05V.

III. The impact of SiC strain on flicker noise and random telegraph noise – new observation &mechanism

The potential impact from SiC strain on flicker noise becomes a critical issue for CMOS oscillator design because that the close-in $1/f^3$ phase noise due to flicker noise up-conversion may become worse. In this paper, flicker noise was measured by using low frequency noise measurement system illustrated in Fig. 3 and expresses by normalized current noise spectral density, denoted as S_{ID}/I_{DS}^2 to ensure a fair comparison. Unfortunately, as shown in Fig. 4(a), the SiC strained nMOS with higher μ_{eff} and I_{DS} suffer the penalty of more than 3 times larger S_{ID}/I_{DS}^2 than the control nMOS, which may lead to increase of close-in $1/f^3$ phase noise due to flicker noise up-conversion and a detrimental impact on CMOS oscillator stability [5]. As for SiC strained nMOS with ultra-small area like W=60nm and L=40nm, the S_{ID}/I_{DS}^2 reveals an interesting feature shown in Fig. 4(b), such as superposition of two Lorentzian functions proportional to $1/f^2$, given one of the corner frequencies, f_c at around 1KHz and another far below the minimum frequency for flicker noise measurement. It means one trap state with shorter τ_c and τ_e resulting in the visible f_c and another slow trap state with very long τ_c and τ_e, thus anomalously low f_c out of the low frequency domain.

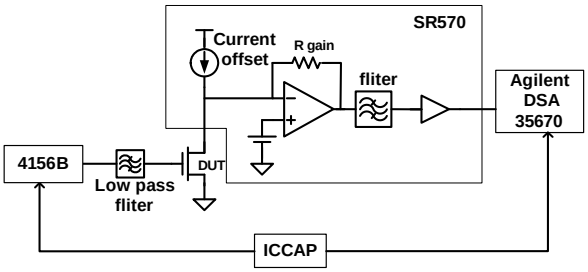

Fig. 3 Low frequency noise measurement system consisting of Keysight dynamic signal analyzer (DSA 35670), low noise amplifier (LNA SR570), and Agilent 4156B for DC power supply. The measurement is automatically controlled by Keysight ICCAP.

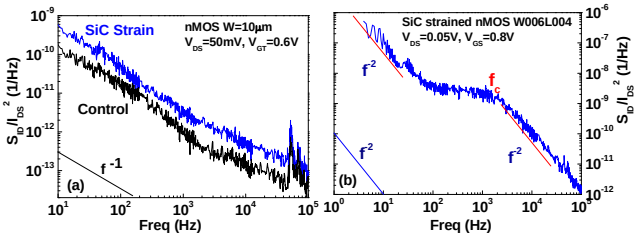

Fig. 4 (a) Comparison of S_{ID}/I_{DS}^2 vs. freq. (V_{GT} =0.6V) measured from SiC strained and control nMOS with W=10μm, L=32.85nm/35.05nm (b) S_{ID}/I_{DS}^2 vs. freq. of SiC strained nMOS with ultra-small area W=60nm and L=40nm

RTN measurement in time domain is a solution to overcome the limitation of minimum frequency in flicker noise measurement, particularly for the investigation of very slow traps with abnormally long τ_c and τ_e. As shown in Fig. 5, the RTN measured from SiC strained nMOS presents a complex spectrum consisting of multiple levels of ΔI_D, which can be decomposed into small- and big-ΔI_D associated with the single- and double- electron traps with very different time constants. For the big-ΔI_D RTN, the τ_c and τ_e are abnormally long to around hundreds of seconds. It means that the trapping/detrapping process of the big-ΔI_D RTN is much slower than that of small-ΔI_D RTN and accounts for the slow traps observed from the Lorentzian distribution with anomalously low f_c at out of frequency domain shown in Fig. 4(b). Further analysis demonstrates two separate groups of τ_c and τ_e corresponding to small-ΔI_D and big-ΔI_D RTN, with more than two orders of gap, shown in Fig. 6(a). Actually, the τ_c and τ_e for either small- or big-ΔI_D RTN are several orders longer than those calculated by elastic tunneling model [7] for the trap depths confined in the ultra-thin gate oxide of 12 Å in the 40nm technology. This new observation from nanoscale devices rules out the elastic tunneling theory and suggests some new mechanisms governing the electrons capture and emission at the oxide or border traps. The time constant ratio, τ_c/τ_e can be derived and given by (3) and the effective trap depth Z_{eff} can be determined by the differential of $\ln(\tau_c/\tau_e)$ w.r.t V_{GS}, according to (4). The results shown in Fig. 6(b) indicate Z_{eff}=6.8Å and 7.2Å associated with small and big-ΔI_D RTN for SiC strained nMOS, and Z_{eff}=5.15Å for control nMOS. Note that the difference of Z_{eff} (ΔZ_{eff}) between the small- and big-ΔI_D RTN in SiC strained nMOS is only 0.4 Å. This negligibly small ΔZ_{eff} cannot explain the dramatic differences of the τ_c, τ_e, and ΔI_D between the small- and big-ΔI_D RTN, according to McWhorter model [7]. Besides, the Z_{eff} confined in the ultra-thin gate oxide of 12 Å behave very shallow trap depth and the transition time calculated by elastic tunneling theory lead to abnormally short τ_c and τ_e to 10^{-9}~10^{-8} s for Z_{eff}=5~7Å, which are more than 10 orders shorter than experimental results (Fig. 6(a)).

$$\ln\left(\frac{\tau_c}{\tau_e}\right)=\beta-\frac{q}{k_BT}\left[\left(1-\frac{Z_{eff}}{T_{ox}}\right)\Psi_S+\frac{Z_{eff}}{T_{ox}}V_{GS}\right] \tag{3}$$

$$\frac{d}{dV_{GS}}\ell n\left(\frac{\tau_c}{\tau_e}\right)=-\frac{q}{k_BT}\frac{Z_{eff}}{T_{ox}} \tag{4}$$

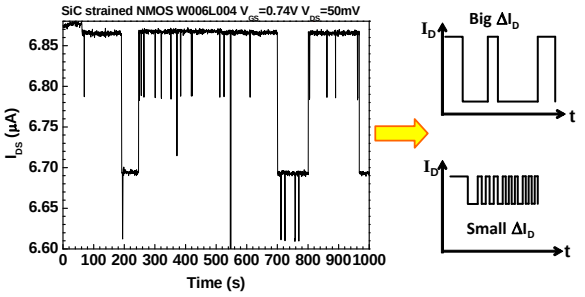

Fig. 5 The complex I_D-RTN spectrum measured from SiC strained nMOS can be decomposed into small and big-ΔI_D RTN.

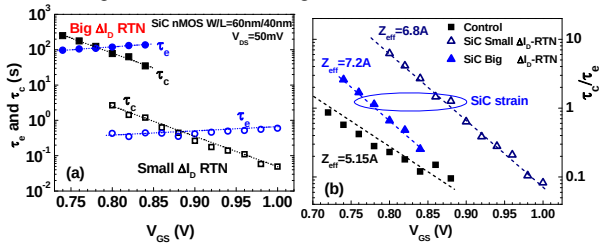

Fig. 6 (a) τ_c and τ_e extracted from small ΔI_D RTN and big ΔI_D RTN measured from SiC strained nMOS at various V_{GS} (b) τ_c/τ_e vs.V_{GS}. Z_{eff} =6.8Å and Z_{eff} =7.2Å extracted from small ΔI_D RTN and big ΔI_D RTN for SiC strained nMOS, and Z_{eff} =5.15Å for control nMOS.

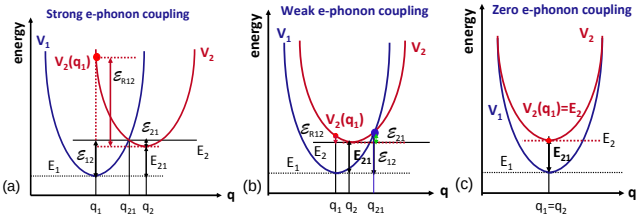

Fig. 7 Adiabatic potentials for the electrons transition between states 1 and 2 (a) strong e-phonon coupling $\varepsilon_{R12} > E_{21}$ (b) weak e-phonon coupling $\varepsilon_{R12} < E_{21}$ (c) zero e-phonon coupling $\varepsilon_{R12}=0$. $\varepsilon_{R12}=V_2(q_1)-V_2(q_2)$. q : reaction coordinate.

In this paper, electron-phonon coupling **[8]** is adopted as a new mechanism to explain the abnormally long τ_c and τ_e, and the dramatic difference between the small- and big-ΔI_D RTN. Fig. 7(a)~(c) illustrate the adiabatic potentials for electrons transition between states 1 and 2 associated with strong, weak, and zero electron-phonon coupling. Herein, $\varepsilon_{R12}=V_2(q_1)-V_2(q_2)$ represents the relaxation energy to be dissipated via the emission of phonons for electrons transition. For strong electron-phonon coupling shown in Fig. 7(a), the significant increase of $\Delta q=q_2-q_1$ and ε_{R12} due to SiC strain can lead to very long τ_c and τ_e according to (5) and (6). Moreover, the τ_c/τ_e as the key factor for extraction of Z_{eff} given by (3)~(4) is independent of ε_R according to (7). The electron-phonon coupling can predict and explain the abnormally long τ_c and τ_e up to above hundreds of seconds for the big-ΔI_D RTN even at very shallow Z_{eff} of around 7 Å in the ultra-thin gate oxide. Besides, this new mechanism can facilitate understanding that the significant difference of τ_c and τ_e between the big- and small-ΔI_D RTN comes from the difference of $\varepsilon_R(\Delta q)$, but the Z_{eff} determined by τ_c/τ_e is independent of ε_R and keeps similar at 7±0.2 Å for the big- and small-ΔI_D RTN (Fig. 6(b)). The $\Delta\varepsilon_R$ between the big- and small-ΔI_D RTN can be calculated by (8), and the result is $\Delta\varepsilon_R$=479±22 meV for this case of SiC strained nMOS.

$$\tau_c=\left(N_c\upsilon\sigma\right)^{-1}e^{\beta(E_C(V_{GS})-E_F)}\cdot e^{\frac{\beta E_{21}}{2}}\cdot e^{\frac{\beta\varepsilon_R}{4}} \tag{5}$$

$$\tau_e=\left(N_c\upsilon\sigma\right)^{-1}e^{\frac{\beta E_{21}}{2}}\cdot e^{\frac{\beta\varepsilon_R}{4}} \tag{6}$$

$$\frac{\tau_c}{\tau_e}=e^{\beta(E_C(V_{GS})-E_F)}e^{-\beta E_{21}}=e^{\beta(E_T(V_{GS})-E_F)} \tag{7}$$

$$\Delta\varepsilon_R=2k_BT\ell n\left(\frac{\tau_{c(Big)}}{\tau_{c(Small)}}\right)+2k_BT\ell n\left(\frac{\tau_{e(Big)}}{\tau_{e(Small)}}\right) \tag{8}$$

IV. Conclusion

SiC strained nMOS with sub-40nm length can realize more than 22% higher μ_{eff} and I_{DS} but reveal the penalty of 3~5 times increase of flicker noise, which will increase close-in $1/f^3$ phase noise and degrade CMOS oscillator stability. The complex RTN spectrum with anomalously long τ_c and τ_e at very shallow Z_{eff} ~7Å in the ultra-thin gate oxide exactly rules out elastic tunneling model. Electron-phonon coupling is adopted as more appropriate mechanism, which can explain and predict the extraordinary increase of τ_c and τ_e due to strong electron-phonon coupling with large relaxation energy, $\varepsilon_R(\Delta q)$ caused by SiC strain. The dramatic increase of flicker noise and RTN appears as a critical issue for low phase noise design when adopting SiC strained nMOS, aimed at SoC with high speed logic and high performance RF/analog.

References

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