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Investigation of Capacitor-less Integrate and Fire Neuron by Using Double Gate PN-Body Tied SOI-FET

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Abstract

Intgrate and fire neuron by using a double gate (DG) PN-body tied (PNBT) silicon on insulator field effect transistor (SOI-FET) was investigated. We found out that the DG PNBT SOI-FET has the integrate and fire function in the single device. It means that it is possible to realize the capacitor-less small footprint neuron circuit with the DG PNBT SOI-FET.

1. Introduction

Importance of artificial intelligence technologies for a highly automated society is growing rapidly. Especially, the artificial neural networks (ANNs) have made remarkable advance owing to progress the deep learning. Recently, spiking neural network (SNN) has been studied for the next generation ANNs. For example, the neuromorphic chip based on the SNN has been developed [1]. Some researchers are focusing on improving the neuron circuit to generate the spikes. The neuron circuit with floating body effects (FBEs) of a silicon on insulator field effect transistor (SOI-FET) is possible to decrease the spike generation power and the footprint of the circuit [2], [3].

In this study, we investigate the integrate and fire neuron by using our newly proposed double gate (DG) PN-body tied (PNBT) SOI-FET [4]. We found out that there is a possibility of the DG PNBT SOI-FET realizing the capacitor-less neuron circuit.

2 Device Structure of DG PNBT SOI-FET

Fig. 1 shows the device structure of the DG PNBT SOI-FET. The device parameters are shown in Table I. We simulated the DG PNBT SOI-FET characteristics by using 3D TCAD HyENEXSS [5]. The DG PNBT SOI-FET has an inherent pnpn thyristor between the source/drain and the body. The first gate and the second gate control the potential of the thyristor base regions. These gates and base regions play roles of carrier integration and ejection described later.

3 Results and Discussions

Fig. 2 shows the DC characteristics of the DG PNBT SOI-FET. The steep slope (less than 2 mV/dec) and the hysteresis characteristics appear. Fig. 3 shows the transient (turn-on) characteristics of the DG PNBT SOI-FET. The DG PNBT SOI-FET has the delay (integrate) time and turns on abruptly. We consider that these characteristics are induced by the floating body effect and the positive feedback on the thyristor [3], [4]. Holes are injected from the body and accumulated under the first gate as shown in Fig. 4 (b). Electrons concentration also increase due to increase the channel potential. When a certain number of carriers accumulate, the pnpn thyristor turns on because of the strong positive feedback and I_d flows abruptly. These characteristics mean the DG PNBT SOI-FET has functions to integrate carriers and to fire at the threshold (strong positive feedback) point. Therefore, we assume that this device can reproduce the integrate and fire neuron without a comparator and capacitors.

Fig. 5 shows the transient characteristics when the pulse voltage which has various widths input. The voltage amplitude V_{amp} and the duty cycle are 1.0 V and 50 % respectively. The pulses are mimic the spike inputs and the device can turn-on even though the intermittent inputs. However, the maximum current depends on the pulse width. Fig. 6 shows V_{amp} dependence when the pulse width is 10 ns. As V_{amp} increase, the number of pulses to turn on decrease. This is because the more carriers inject from the body to the first gate region when the higher V_{amp} biases. These characteristics mean that the frequency of the fire can be controlled by V_{amp}.

I_d turns on continuously after the first turn-on as shown in Figs. 5 and 6. Carriers remain in the base regions after turn-on. The carrier accumulation condition must be reset for reproducing the single spike neuron function. We propose the way to eject carriers as shown in Fig. 7 (a). The reset signals (0 V) are input to the body and the second gate if I_d larger than a threshold current. The accumulation carriers eject to the body and the base conditions are reset. Fig. 7 (b) shows the I_d when the reset signals are input. I_d does not turn on continuously after the reset. We confirmed that the DG PNBT SOI-FET can also make the single spike signal.

4. Conclusions

We investigated the integrate and fire neuron by using the DG PNBT SOI-FET. We found out that the DG PNBT SOI-FET has the function to integrate carriers and fire without comparator and capacitors. We showed that the device can generate the continuous spike and also the single spike signal with the reset. It means that it is possible to realize the small footprint neuron circuit with the DG PNBT SOI-FET.

Acknowledgement

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References

[1] P. A. Merolla *et al.*, *Science* (2014) 668. [2] S. Dutta *et al.*, *Sci. Rep.* (2017) 8257. [3] M.-W. Kwon *et al.*, *IEEE J-EDS* (2019) 1080. [4] T. Mori *et al.*, *SISPAD* (2019) 291. [5] HyENEXSS^{TM} ver5.5, Selete (2011).

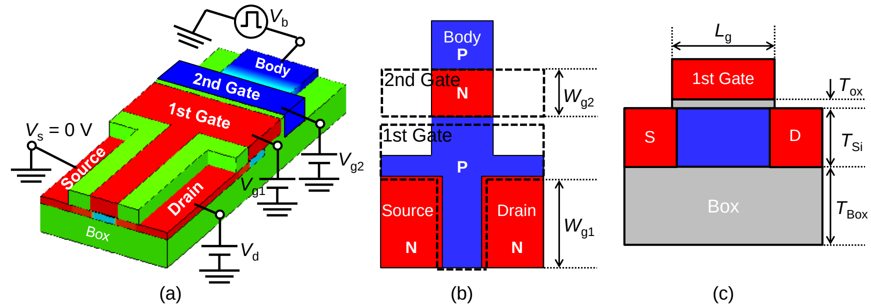

Fig. 1 Device structure of the PNBT SOI-FET. (a) Top-down view. (b) Top view. (c) Front view.

Table I Device parameters.

Device Parameter	
Gate Oxide T_{ox}	5 nm
SOI Thickness T_{Si}	50 nm
Buried Oxide Thickness T_{Box}	200 nm
Gate Length L_g	200 nm
1st Gate Width W_{g1}	1 µm
2nd Gate Width W_{g2}	200 nm

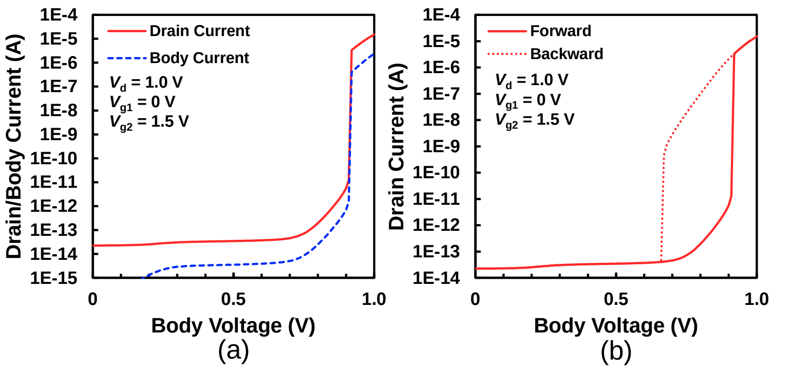

Fig. 2 DC characteristics of DG PNBT SOI-FET. (a) I_d, I_b–V_b characteristics, (b) double sweep characteristics.

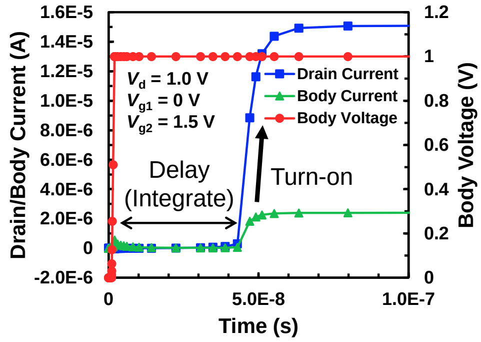

Fig. 3 Transient (turn-on) characteristics of DG PNBT SOI-FET.

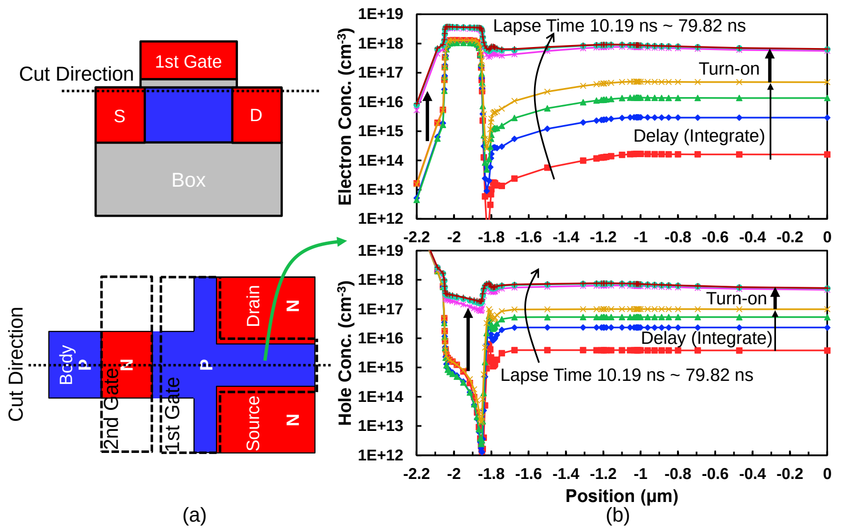

Fig. 4 State of carrier integration. (a) Cut direction. (b) Carrier concentration between integrate and turn-on.

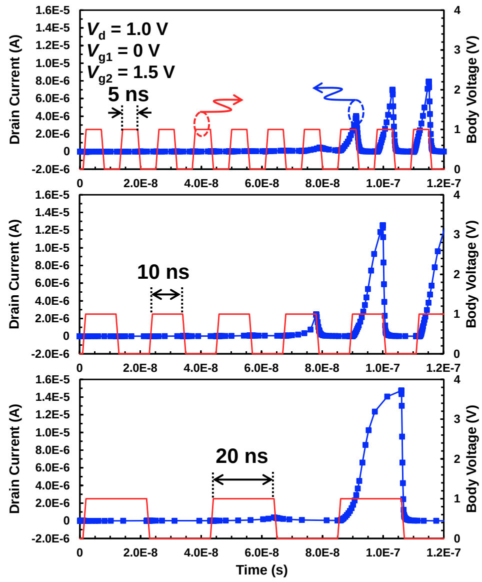

Fig. 5 I_d dependence on pulse width.

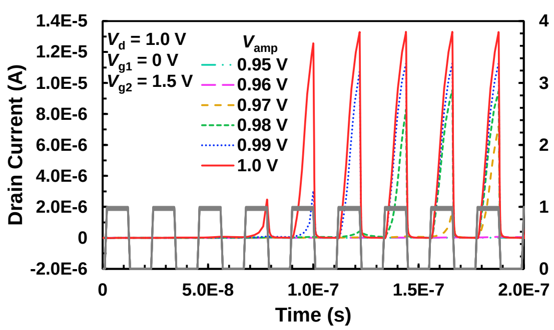

Fig. 6 I_d dependence on pulse amplitude.

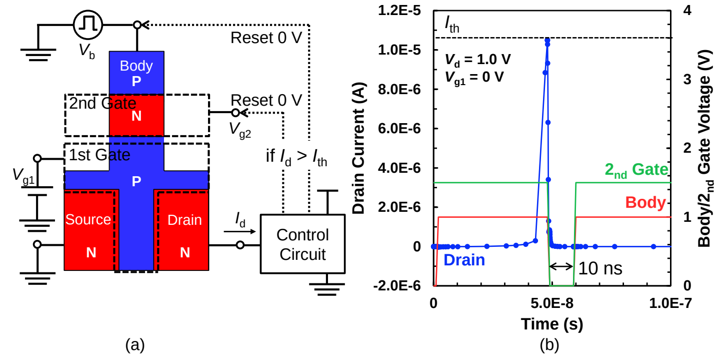

Fig. 7 Spike generation with reset action. (a) Reset circuit. (b) I_d dependence on time with reset action.