Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp37-38

On-Wafer Recorders for Assessing Wide Range Plasma Induced Charging Effect in FinFET Processes

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Abstract

Newly proposed on-wafer test patterns for assessing wide-range plasma induced charging levels in advanced FinFET logic processes have been demonstrated. By sizing up the capacitor linked to the antenna node, the maximum sensing level can be extended successfully.

Introduction

In recent years, the continuous evolution of semiconductor process technology pushes key circuit elements to scale down aggressively. Advanced CMOS FinFET processes include many more plasma-etching steps, enabling the formation of high aspect ratio structures [1]. Meanwhile, as the intensity of plasma and the number of processing steps with plasma raise, plasma induced damage becomes more serious in FinFET circuits.

Design rules which restrict the size of metal layer structures to avoid plasma charging exceed the tolerance level are commonly used to practice in the industry [2]. Adding protective diodes [3] in parallel to a long wiring patterns can also help shunt the charging current from the transistors. These methods reduce design flexibility on structures pro to plasma induced damages.

Previous studies [4-6] report an on-wafer plasma induced charging effect detector demonstrated in advanced FinFET technologies. In order to widen the sensing range, the effect of adding different types and sizes of capacitors next to the PID detector is investigated in this work. A series of detector patterns targeting a wide range sensing are incorporated in on-wafer test-lines for monitoring the plasma processing conditions.

Operation Principle and Test Pattern Design

A 3D illustration and layout with the parasitic capacitances which seeing from the antenna node of a plasma induced damage recorder structure are outlined in *Figure 1*. The total capacitance on the antenna is composed of capacitance from antenna to substrate and floating gate, respectively. *Figure 2 (a)* shows the total capacitance of the antenna with raising antenna ratio. From the detectors with increasing antenna area, the distribution of threshold voltage distributions of the PID recorder across a 12-inches wafer are compared in *Figure 2 (b)*. As antenna area raises, the amount of charge collected increases, leading to more significant threshold voltage shifts.

The basic operation principles of the PID detect/record device is explained on the flow chart in *Figure 3(a)*. The detecting mechanisms, starting with the charging of antenna to the final change of threshold voltage of the recorders can be described by simple charging and FN tunneling equations. *Figure 3(b)* lists all parameters used in the model correlating ΔV_t with plasma flux seen by the antenna. *Figure 4* shows that large antenna area leads a saturated antenna potential, V_{ant}, causing a maximum detection limit. To avoid saturation when plasma flux level exceeds the detector limit, antenna capacitance is deliberately increased by adding C_L. To modify the charging rate on the detector's antenna during plasma processes, additional loading capacitor, C_L, for reading the sensitivities of the plasma detector is proposed. *Figure 5* illustrates all the possible capacitance on the FG-based PID detector with C_L. Three types of C_L implemented are MIM capacitor, STI capacitor, and sidewall capacitor, as shown in *Figure 6(a)*. The capacitance per unit area/length summarized in *Figure 6(b)* suggest that MIM capacitor seems to be the most area-efficient type for extending C_{tot}.

Experimental Results and Discussion

Figure 7 compares the simulated parasitic and total capacitance when different loading capacitors are added. More prominent effect on the total antenna capacitance is found for detector with AR ratio under 1000. Drain current characteristics of the PID recorder with different levels of C_L are compared in *Figure 8(a)*. *Figure 8 (b)* further shows that the size of total capacitance of the antenna directly affects the measured threshold voltage shifts. For samples with low antenna ratio, the total capacitance is dominated by C_L. Antenna potential calculated based on ΔV_t through the model in Figure 3 is plotted against C_{tot}. A strong correlation suggested that under the same plasma flux, V_{ant} can be effectively reduced, preventing saturation of the detection response. Recorded threshold voltage shifts from samples across wafer with different sizes of MIM loading capacitors with AR=1K are compared in Figure 10. By increasing $C_{L,}$ one can effectively attenuate the responsivities and extend the sensing range of the PID detector, as projected in Figure 11.

Conclusion

Plasma induced damage detector can be further optimized by connecting additional loading capacitors. The new designs allow for wide-range sensing of plasma charging levels in advanced IC processes.

Acknowledgements

The authors would like to acknowledge the support from Taiwan Semiconductor Manufacturing Company (TSMC) and Ministry of Science and Technology (MOST), Taiwan.

References

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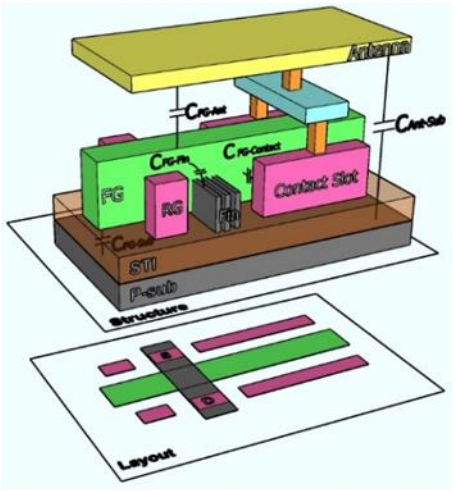


Figure 1. 3D schematic illustrating the parasitic capacitance seen from the antenna structure in a PID recorder.

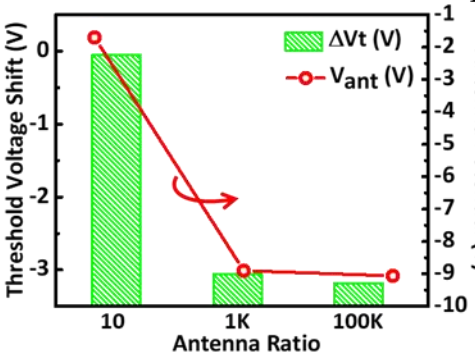
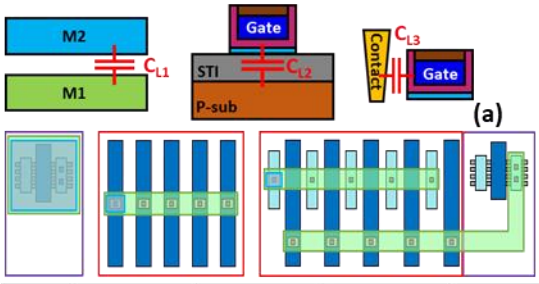


Figure 4. Increasing antenna area leads to saturated Vt level on the detectors, while V_{ant} saturates.



C_P	C_{Ant}	C_{L1}	C_{L2}	C_{L3}
0.95 fF	0.025 (fF/μm^2)	0.354 (fF/μm^2)	0.062 (fF/μm^2)	0.125 (fF/μm)

Figure 6. Loading capacitors realized by different structures as illustrated in the (a) cross-sections and corresponding layouts. (b) Capacitance per unit area/length on these three types of C_L designs.

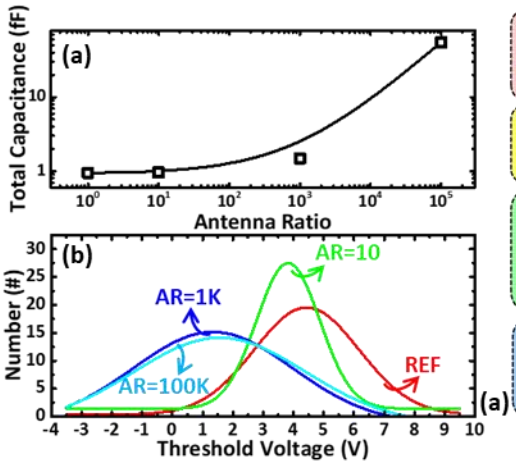
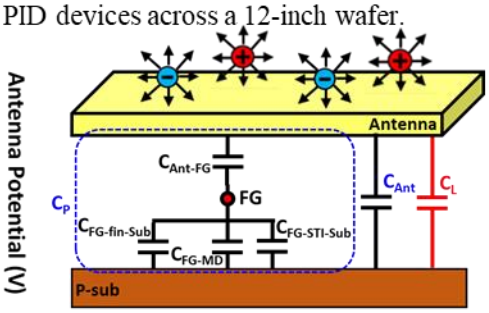


Figure 2. (a) Total capacitance of the antenna with raising AR. (b) Distributions of measured threshold voltage from the PID devices across a 12-inch wafer.



$$C_{tot} = C_P + C_{Ant} + C_L$$

Figure 5. Compositions of capacitance on an antenna structure with additional load capacitor, designed to tone-down the sensitivities of the plasma detector.

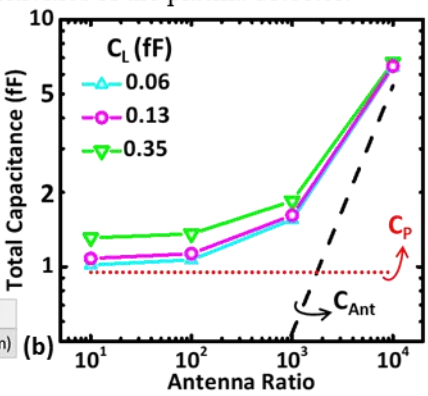
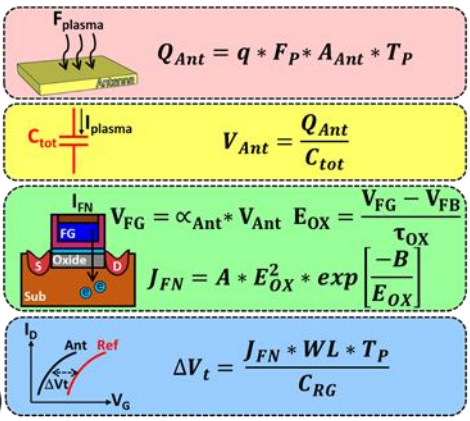


Figure 7. Parasitic and total capacitance as different levels of load capacitances are added.



(b)

Q_{Ant}	Charges on the antenna	Coul
F_P	Plasma flux	A/cm^2
A_{Ant}	Antenna collection area	cm^2
T_P	Plasma process time	s
V_{Ant}	Antenna potential	V
V_{FG}	Floating gate voltage	V
$\propto_{Ant}$	Coupling ratio of antenna	X
E_{OX}	Oxide electric field	V/cm
V_{FB}	Flat band voltage	V
τ_{OX}	Oxide thinkness	cm
J_{FN}	FN tunneling flux	A/cm^2
ΔVt	Delta threshold voltage	V
WL	Oxide effective area	cm^2
C_{RG}	Read gate capacitance	X

Figure 3. (a) Detecting mechanisms, starting with the charging of antenna to the final change of threshold voltage of the recorders. (b) List of parameter descriptions.

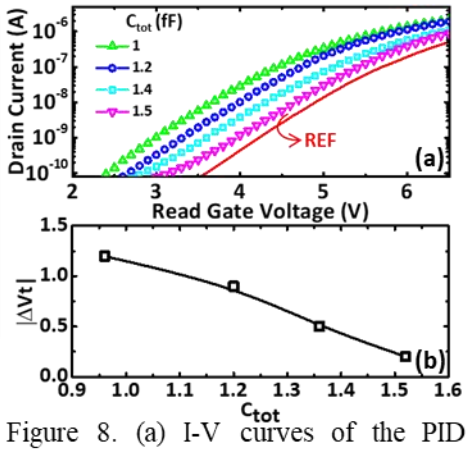


Figure 8. (a) I-V curves of the PID recorders with different levels of C_L . (b) Total capacitance of the antenna directly affect the final threshold voltage shifts.

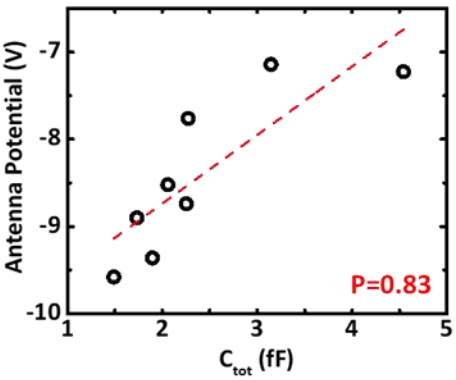


Figure 9. Projected antenna potential during plasma charging vs. the total antenna capacitance on 80 of samples.

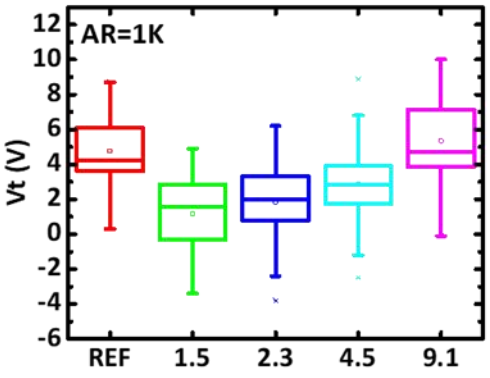


Figure 10. Box chart of final Vt on the detectors with MIM capacitors of increasing C_L level.

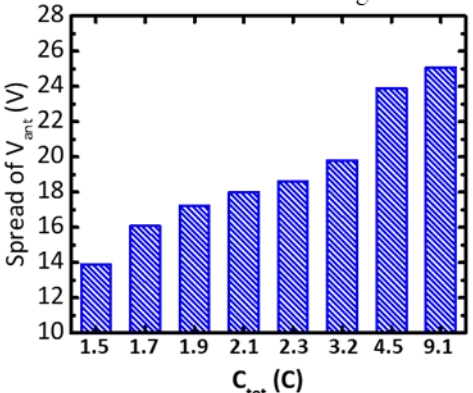


Figure 11. Maximum V_{ant} across a wafer are effectively widen when C_{tot} increased by C_L.