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White Spots Caused by Junction Leakage in Small Pixels of CMOS Image Sensor

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Abstract

White spots caused by junction leakage in 0.8μm CMOS image sensor (CIS) pixel were analyzed and improved. A strong electric field induced at the junction of photodiode and nearby transistors in a highly shrunken pixel makes leakage current which might cause long-term reliability problems as a type of white spots. In order to mitigate the electric field, layout, doping concentration, and heat process of pinned photodiode (PPD) were simulated and optimized. As a result, it was found that these factors affect junction leakage near photodiode which depends on the operating voltage. By the optimization of the electric field, the voltage dependent white spots were completely removed and the 0.8μm pixels were successfully employed to the mobile CMOS image sensor.

1. Introduction

Recently, smartphones have been positioned as electronic devices that replace the traditional cameras. Therefore, strong demands of better image quality have been continuously increased for the smartphone cameras and CISs. Especially, low-light image performances and long-term reliabilities of small pixels for high-resolution have been considered as key success factors.

As pixel pitch has been shrunken down to the submicron region for the implementation of high-resolution sensor in a limited pixel area, many efforts have been made to overcome the technical barriers such as small full well capacity (FWC), large crosstalk, and etc. [1][2]. However, junction leakage and related reliability problem by the strong electric field due to the closer PN junction in a small pixel area have not been reported yet. In this paper, the white spots caused by junction electric field which depend on the operating voltage and might cause long-term reliability problems were analyzed and optimized. In addition, several solutions of pixel design and process were suggested.

2. Simulation and Experimental Results

In order to improve image quality at low light conditions, it is required to reduce dark current and white spots. So, removal of shallow trench isolation (STI) can be a good approach for the low dark current and white spot which come from STI interfaces. Furthermore, since photodiode (PD) and transistors (transfer gate and reset gate, row select switch) for pixel operation should be located within a small pixel area of 0.8 x 0.8 μm^2, STI less structure is helpful to obtain efficient layout as well as low dark current [3]. But, the increase of electric field between PPD and transistor is inevitable compared to the big pixel.

As shown in Fig. 1 (a), in general, dark current of the PPD with 4-TR structure is mainly generated in the PD, STI and the deep trench isolation (DTI) interface regions [4]. However, as the pixel size gradually decreases, it is expected that junction leakage also contributes on the deterioration of dark current because of electric field. Fig. 1 (b) shows the pixel layout without STI. Because the P- and N- type doped regions are closely placed in the small pixel area of 0.8um pitch, strong electric field is induced between VDD and PPD when the high VDD is applied. The electrons flow into the PD through this abrupt junction.

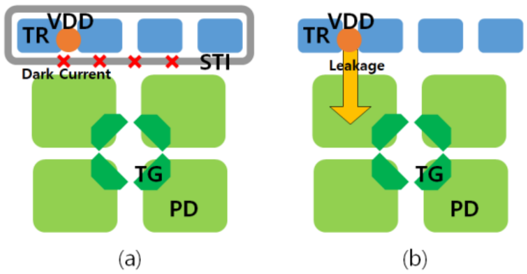

Fig. 1 (a) Pixel layout with STI and (b) without STI

Fig. 2 (a) shows the output changes of the pixels as the operating voltage increases. As shown in this figure, two kinds of white defects are observed. Some types are white defects which are voltage independent (type1) and the other types are white defects whose output varies by operating voltage (type2). When integration time of PD is 0ms, both two types of defects showed little change in their output. Therefore, type2 defects depend on the operating voltage and integration time. On the contrary, type1 defects depend on only integration time. Thus, the above two types of white defects have different mechanisms of defect generation. The electrons that contribute to white spots in type1 pixels are generated in the PD and DTI interface as mentioned above. These defects are well-known white spots that are not increased by the operating voltage. Type2 pixels are white spots caused by induced strong electric field with applied high voltage to the junction near VDD node. The electrons flow into the PD through abrupt junction which causes the defective signal of sensor in the dark condition. These white spots might cause the long-term reliability problems, because the output of defects is proportional to the applied voltage level and duration time.

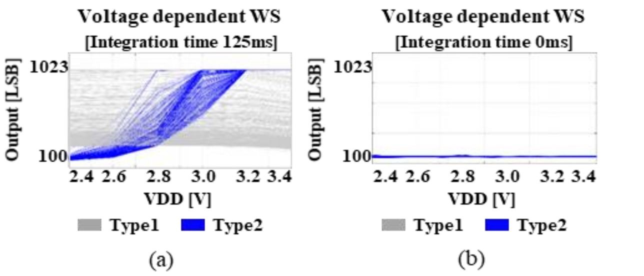

Fig. 2 pixel outputs according to VDD voltage under (a) integration time of 125ms and (b) 0ms.

Layout and process conditions have been investigated through simulation to reduce the electric field. On the technology computer-aided design (TCAD) simulation, PPD doping concentration and distance between PPD and VDD were changed to find the optimum condition. As shown in Fig. 3, TCAD simulation of electric field between PD and transistors were carried out. The results showed the correlation between white spots and electric field at the junction. The electric field could be mitigated with increasing distance between PPD and VDD as shown in the Fig. 3 (a). In addition, the change in electric field is shown in Fig. 3 (b). The electric field is reduced as doping concentration of PPD decreases.

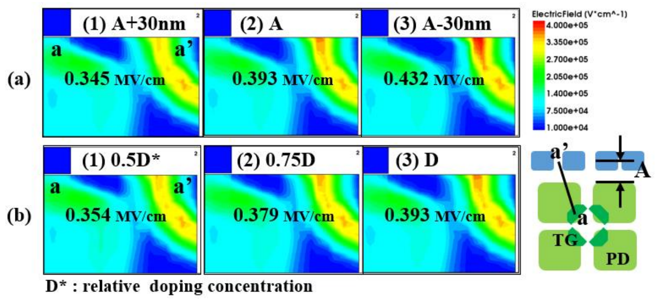

Fig. 3 Simulated results for electric field according to (a) distance between PPD and VDD node and (b) doping concentration of PPD.

Based on the simulation results, the pixel of 0.8um pitch could be designed without junction leakage. Fig. 4 (a) shows the experimental results that the number of voltage-dependent white spot could be improved by expanding the distance between PPD and VDD node. With an increase of 35nm distance, the number of voltage-dependent white spot was drastically reduced by 96%. As shown in Fig. 4 (b), white spots related to junction leakage could also be reduced by lower PPD doping. As the PPD doping was decreased by 38%, the number of voltage-dependent white spot was also reduced by 80%. Additional optimization of heat process was employed to suppress the diffusion of P and N type impurities. Generally, as the heat process is added after ion implantation (IIP) process, the Si interface is cured and the number of normal white spot decreases (type1). However, adding the heat process affects the strong electric field in the small pitch pixel. Therefore, white spots were also improved by lowering temperature in the silicon process (type2).

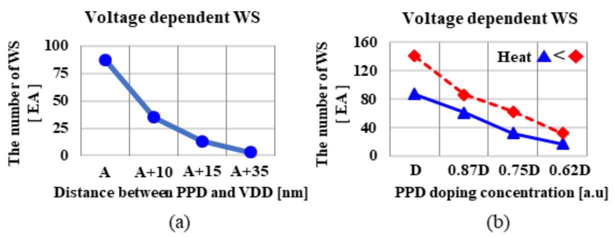

Fig. 4 Measurement results for number of white spots according to (a) distance between PPD and VDD node, (b) doping concentration of PPD and temperature in the silicon process

By the optimization of layout, doping concentration and heat process, the number of white spot was not changed after high-temperature operating life (HTOL) reliability test as shown in Fig. 5. In other words, type2 white spots were completely removed.

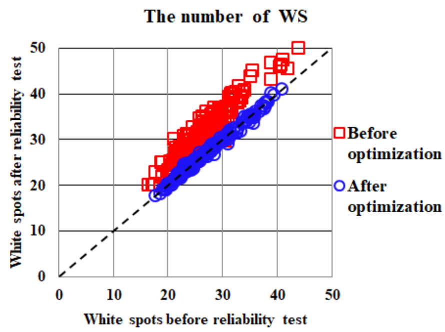

Fig. 5 Comparison in the number of white spot between before- and after-HTOL reliability tests

3. Conclusions

In summary, the white spots caused by the junction leakage of CIS with 0.8 μm pitch pixel were analyzed and improved. In the developing small-size pixel without STI, white spots generated by strong electric field need to be reduced for long-term reliability of sensor. Expanding the distance between PPD and VDD node, lowering the doping concentration of PPD and process temperature can improve white spots. As a result, the solutions to reduce electric field and white spots demonstrated by simulations and experiments are successfully employed to mobile CIS sensor with 0.8 μm pixels.

References

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