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Towards extreme scaling of logic standard cells using Forksheet devices

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Abstract

Scaling below 3nm will bring far into the post FinFET era where extremely scaled logic standard cell heights and SRAM will limit the nanosheet scalability. We propose the novel forksheet device architecture as ultimate scaling device towards 2nm and beyond. The unique device architecture substantially reduces p-to-n space and thereby offers performance improvements over nanosheet due to increased area efficiency and reduced FEOL parasitics.

1. Introduction

CMOS scaling driven by metal and gate pitch scaling determines to a large extend the chip area for both logic and SRAM [1]. Several pitch scaling challenges have emerged posing limitations to cell scaling. Issues due to a steep increase in BEOL resistance with Cu metallization can be mitigated by using barrier-less metals e.g. Ruthenium and high aspect ratio lines with airgap have been introduced [3]. Gate pitch scaling, associated to channel control and contact resistance, has a more fundamental issue which is difficult to overcome. Consequently, to compensate for the lack of gate pitch scaling, cell height reduction was proposed since the 10nm node [4]. This structural scaling has focused research on new challenges such as scaling boosters to improve secondary design rule, place and route innovation to tackle pin congestion and device innovation for better drive vs. parasitic trade-offs. The promising forksheet device (FSH) addresses those key challenges to enable scaling towards 2nm and beyond [5,6] (Fig. 1). It allows for aggressive p-to-n scaling for low track height standard cells (Fig. 2) and eliminates gate extension for SRAM cells (Fig. 3).

2. Forksheet as scaling booster for standard cell PPA

Fin depopulation to 2 fin devices to accommodate cell track height scaling down to 6 track is a common adoption within industry down to 3nm. Scaling to 5 tracks is made possible by moving towards buried power rails and relaxing the MOL design rule arc associated to power rail taping. However, further fin depopulation towards single fin architecture needed for 5T proves difficult due to variability and performance drop not recoverable with fin height increase [2]. Nanosheet (NSH) Gate All Around (GAA) devices [7,8] offering a better drive per area footprint can maintain performance down to 3nm. The window of performance improvement over single fin is however closing at 2nm. In this context FSH device is expected to provide further NSH scalability beyond 2nm. The FSH device consists of vertically stacked lateral sheets having a forked gate structure on one side and a dielectric wall on the other side (Fig. 4). For GAA devices p-to-n separation is driven by mask overlay, work function engineering, well implant and the risk of merging P and N epitaxially grown source and drain (EPI). In the FSH, the dielectric wall between N- and PFET can act as a natural barrier to self-align both the gate and contact providing a solution to the fundamental challenge of their integration at scaled dimensions. Furthermore, from the electrical perspective, it results in a reduced gate to contact capacitance and enables reduced p-to-n separation. These aspects are combined to form interesting standard cell architectures. Firstly, the reduced capacitance offers performance boost which is enhanced using a MOL optimized architecture creating a Ceff optimized layout. Secondly, the reduced PN space can be utilised to either allow an increase in the active area resulting in an Ieff optimized layout or to reduce the cell height down to 4.3T resulting in an area optimized layout (Fig. 5). The performance gain at iso-power is up to ~10% on the circuit benchmark including MOL/BEOL parasitics using the Ceff layout. Additional ~5% peak performance boost using Ieff is observed. Fig. 7 shows the capacitance breakdown for various cell architectures.

3. Process flow challenges and device opportunities

The FSH process flow is very similar to the NSH flow [7] with limited added complexity (Fig. 8). For the wall formation material choice is important for electrical performance and material integrity throughout the flow. The dielectric wall can be formed after patterning the Si/SiGe superlattice by spacer deposition and etch back. The thickness of the top sacrificial SiGe layer sets wall height above the top Si channel impacting the inner spacer deposition [9, 10]. While the FSH device has its own challenges it also leaves room for further device optimization. As a tri-gate structure it will naturally exhibit worse subthreshold slope compared to GAA. However, this can be partially recovered using a selective channel recess forming a Pi-gate structure (Fig. 9). However, this results in effective width reduction compromising drive strength. Therefore, a key challenge for future FSH evaluation is to improve device performance while finding the right balance between Weff and short-channel control.

3. Conclusions

We have proposed the FSH architecture as the ultimate scaling of a 2D device towards 2nm. It can provide further improvement of area and performance by reducing n-to-p spacing. The advantage of the FSH can translate into either cell scaling down to 4.3T or enhanced performance.

References

[1] Liebman L. et al, VLSI 2016; [2] Garcia Bardon M. et al, IEDM 2016; [3] Baert R. et al, IITC 2020; [4] Ryckaert J. et al, IEDM 2019; [5] Weckx P. et al, IEDM 2017; [6] Weckx P. et al, IEDM 2019; [7] Mertens H. et al, IEDM 2016; [8] Loubet N. et al, VLSI 2017; [9] Barraud S. et al, IEDM 2016; [10] Loubet N. et al, IEDM 2019;

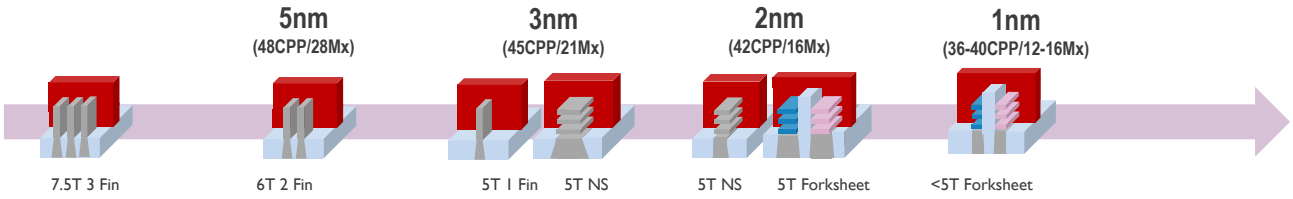

Fig. 1. Extending roadmap beyond nanosheet (NS) where gate pitch scaling saturation requires St cell Track height (T) scaling boosters.

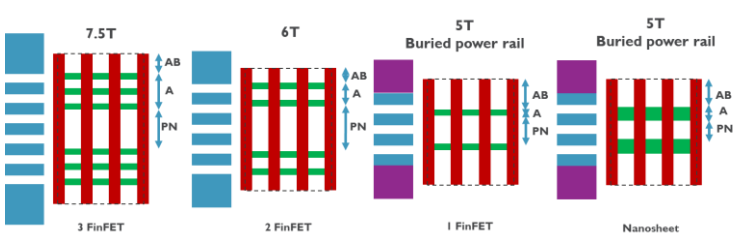

Fig. 2. the PN space becomes the main bottleneck for logic track height scaling. 6T is enabled by fin depopulation while further scaling to 5T requires buried power rials.

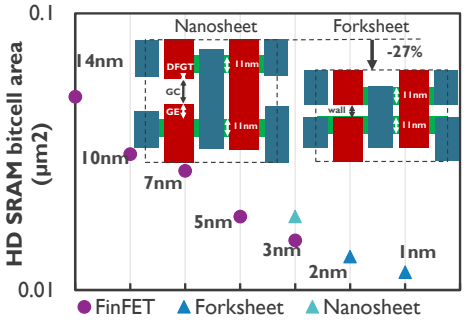

Fig. 3. For SRAM bitcell scaling the gate cut and gate extension in PN becomes main bottleneck (first PN, then SRAM scaling_

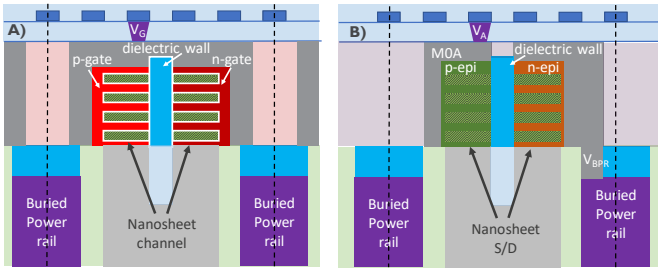

Fig. 4. FSH device architecture shown along a) the gate trench and b) the S/D trench. The FSH dielectric wall separates p and n device

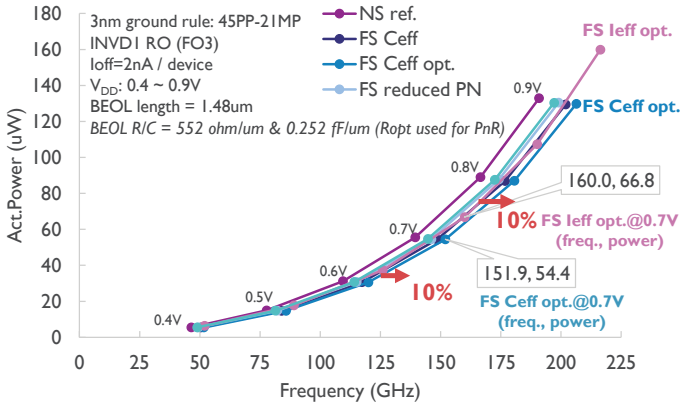

Fig. 6. Using a Ceff optimized architecture the performance gain at iso-power up to ~10% on the circuit benchmark including MOL/BEOL parasitics.

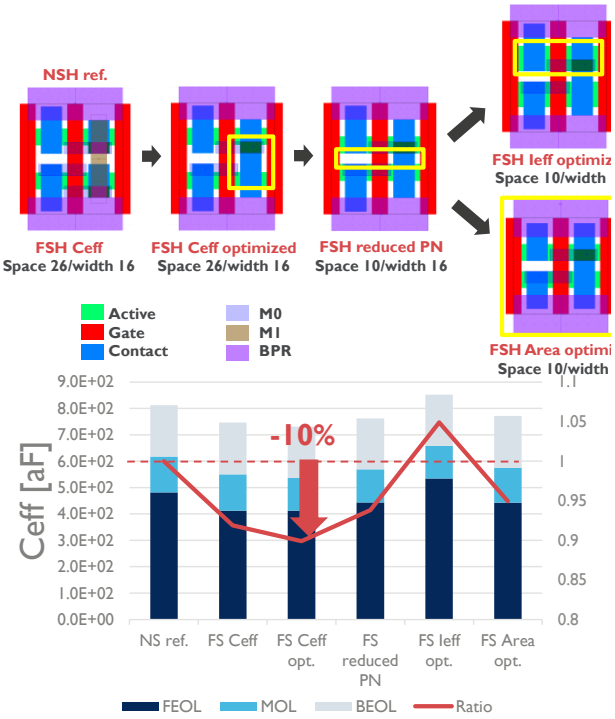

Fig. 7. Breakdown of Ceff contribution indicates that the Forksheet device offers substantial lowering of FEOL capacitance.

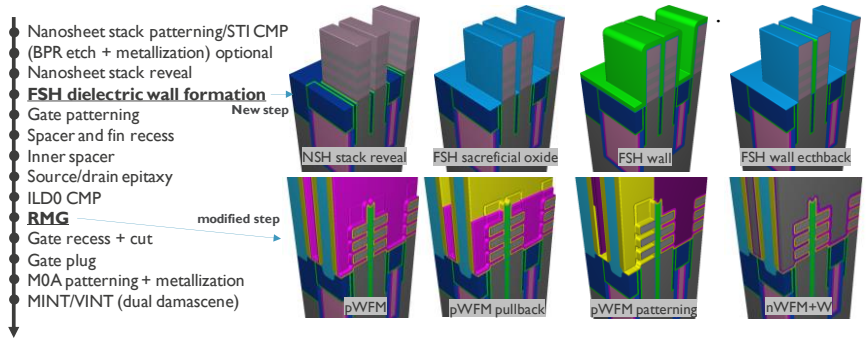

Fig. 8. Forksheet process flow uses the backbone of the nanosheet flow with an added module for dielectric wall formation and modified RMG step.

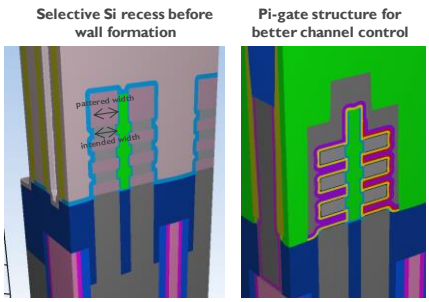

Fig. 9. Selective channel recess before wall formation creates Pi-gate structures for better channel control.