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Evaluation of the impact of source/drain epi implementation on logic performance using combined process and circuit simulation

Assawer Soussou[1], Tom Schram[2], Kenichi Miyaguchi[2], Ivan Chakarov[1], Bertrand Parvais[2] and Joseph Ervin[1]

[1] COVENTOR
3 Avenue du Québec, 91140 Villebon sur Yvette, France
135 Beaver Street, Waltham, Massachusetts, United States
E-mail: asoussou@coventor.com
[2] IMEC
Kapeldreef 75, 3001 Heverlee, Belgium
E-mail: Tom.Schram@imec.be

Abstract

In this paper, we explore an end-to-end solution using SEMulator3D® [1] to address the need to include process variation effects in circuit simulation. For the first time, we couple SEMulator3D with BSIM compact modeling to evaluate process variation impacts on circuit performance. The process integration goal of the study was to optimize contacts and spacer thickness of advanced-node FinFETs in term of speed and power performance. To do so, we compare three structures with different spacer recess levels and epi shape growth profiles. We investigate the effect of low-k spacer thickness variation to select the best combination of spacer thickness and S/D epi shape to improve speed and power performance.

1. Introduction

In a previous study [2], we used Coventor SEMulator3D, a virtual platform for advanced manufacturing processes simulation, to perform RC and drift diffusion (DD) calculations and forecast performance (delay, energy, power) of a 5 nm node inverter. Deposited spacer thickness of 3-10 nm and a gate length variation from 14-18 nm were evaluated [2].

In this study, we will use SEMulator3D to perform process simulation and RC netlist extraction. The RC netlist will be used with BSIM compact models [3] to perform a Spectre® circuit simulation [4]. Using this methodology, we will explore the effect of process variation on speed and power performance. An inverter with three different epitaxy (epi) growth shapes and spacer recess levels with various spacer thicknesses will be compared.

2. Methodology

Fig. 1 illustrates the end-to-end solution proposed in this study to address considering process variation effects requirement, fully captured using SEMulator3D, in circuit simulation. We used three software: SEMulator3D, BSIM compact model and Spectre circuit simulation. Starting from the GDS with pins and label for contact annotation, we used SEMulator3D for process simulation and RC netlist extraction. SEMulator3D extracted 3D geometric output parameters using virtual metrology and 3D parasitics of middle-of-line (MOL), epi and M1 for annotated RC netlist. The complete netlist based on SEMulator3D extractions coupled with BSIM compact model simulation of front-end-of-line (FEOL) enabled Spectre circuit simulation, to obtain speed and power performances for the three inverters.

3. Simulations

Process simulation

Process flows of the three structures were simulated using SEMulator3D up to the M1 metal level. Fig. 2 displays key process steps and highlights the process difference between the three inverters for PMOS. After CMOS RMG and low-k spacer formation, the parasitic spacer formed around the fin is partially or fully recessed prior to source and drain (S/D) epi growth. The spacer was completely etched for structure 1 and partially etched for structures 2 and 3. After the spacer etch and the Si fin recess, selective S/D epi was grown [5]. Simulated epi shapes for each structure are shown in Fig. 2. For structures 1 and 2 the epi is merged, while it is not merged for structure 3. The S/D epi process flow was adapted to obtain the same epi-shape for both NMOS and PMOS.

An inverter annotated layout assuming 24 nm fin and 48 nm gate pitches with 18 nm gate length was used for the process model. Contact labels in the GDS layers masks for metal interconnection, via, gate and fin (Fig. 3) were also included.

For each inverter structure, 33 process simulations were performed varying the final low-k spacer thicknesses from 3.5 nm to 8.5 nm for NMOS and PMOS. Gate length, fin height and thickness, gate oxide thickness and capacitance were calculated for the inverters and structures. Complete netlist files were generated for Spectre circuit simulation.

Compact modeling

We used a BSIM device model for intrinsic device modeling including S/D diffusion and channel effects. We assumed an abrupt dopant diffusion with zero overlap at the metal gate level and constant potential at the epi and fin interface. Compact model approximations were verified using SEMulator3D drift diffusion simulations.

Circuit simulation

The compact model was based upon a BSIM device model for the 5 nm node. The BSIM model, coupled with

the complete netlist extracted using SEMulator3D, enabled a complete Spectre circuit simulation.

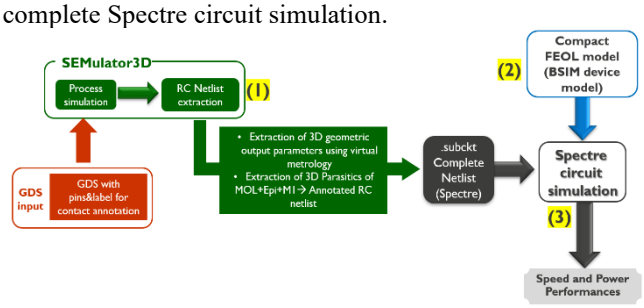

Fig. 1 Flow diagram illustrating the methodology of this study.

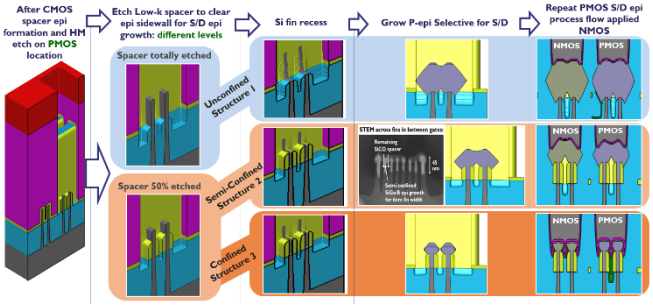

Fig. 2 Key process steps comparison of the three structures.

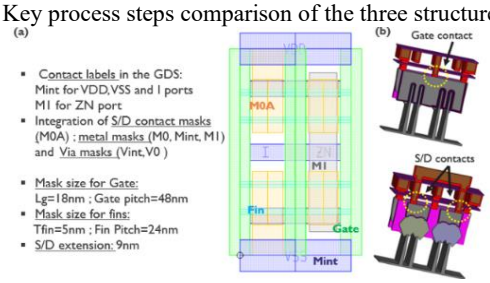

Fig. 3 Design structure (a) and gate and S/D contacts (b).

2. Speed and power performances

Fig. 4 compares the plot of power as a function of frequency obtained for the three structures. The impact of spacer thickness and VDD variations on power performances was also investigated (Fig. 4). For each VDD, we noticed a similar power-speed trend for all epi shape geometries: increasing spacer thickness induced a decrease in power. Hence, to compare epi shape geometries, the remainder of the study was focused on VDD=0.7V power-speed analysis (Fig.4 (b)). For each epi geometry, there was an optimum spacer thickness that produced maximum speed and optimum (Reff×Ceff). For all spacer thicknesses, at a similar power performance, epi shape confined structure 3 offered the highest speed.

Fig. 5 displays S/D access resistances (S/D-R) and Gate-to-S/D (GT-S/D) capacitances for the three structures at 6.5 nm optimum spacer thickness for both NMOS and PMOS. Structures 1 and 2 have close S/D resistances as they have a similar S/D epi shape. Keeping a low-k spacer for semi-confined structure 2 induced a lower GTD capacitance. Semi-confined and confined structures 1 and 2 have similar GTS and GTD capacitances as they have equivalent low-k spacers.

For confined structure 3, we noticed lower S/D-R as S/D contact surface is larger and closer to the fin.

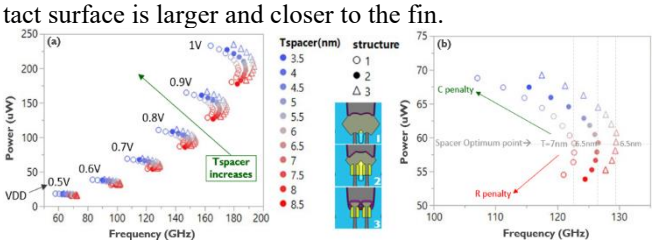

Fig. 4 Power-Speed plot comparison for three inverters at a VDD varying from 0.5V to 1V (a) and enlarged VDD=0.7V result (b).

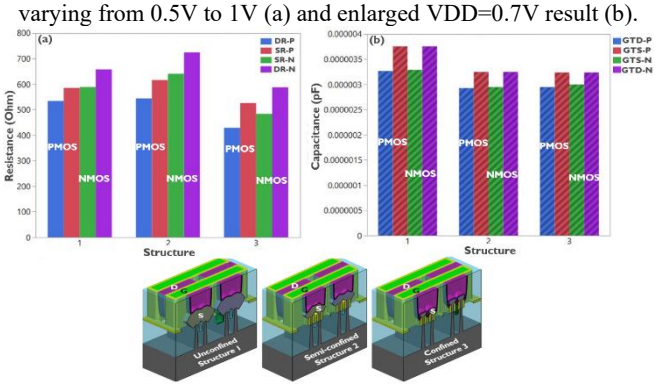

Fig.5 S/D access resistances (a) and Gate-to-S/D capacitances (b) at 6.5 nm optimum spacer thickness for both NMOS and PMOS.

2. Conclusions

In this paper, we delivered an end-to-end solution providing valuable insight into device and circuit performance impacts from process and integration options. We demonstrated a flow enabling process simulation variation using SEMulator3D to be coupled with BSIM compact modeling and included in circuit simulation via RC netlist extraction. The effect of process flow variation across three different inverter S/D epi shape geometries using different spacer recesses were successfully evaluated and compared. The impact of VDD and low-k spacer variations on speed and power performance was also explored.

For all spacer thicknesses, the highest speed was obtained for epi shape confined structure 3. Increasing spacer thickness induced a decrease in power. A spacer thickness equal to 6.5 nm provided the optimum value for power and speed performance using structure 3. Confined structure 3 having the S/D contact surface larger and closer to the fin produced lower S/D-Resistance, compared to the unconfined and semiconfined structures 1 and 2. Maintaining a low-k spacer for semiconfined and confined structures 2 and 3 provided lower and similar GTS and GTD capacitances than seen in structure 1.

References

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