Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp47-48

Variability and Corner Effect of GAA p-Type Poly-Si Junctionless Nanowire/Nanosheet Transistors

Min-Ju Ahn, Takuya Saraya, Masaharu Kobayashi and Toshiro Hiramoto
Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba Meguro, Tokyo, 153-8505, Japan
Phone: +81-3-5452-6264 E-mail: mjahn@nano.iis.u-tokyo.ac.jp (fhfjdk@gmail.com)

Abstract

V_T Variability of and corner effects in gate-all-around GAA p-type poly-Si junctionless nanowire (NW)/nanosheet (NS) transistors are discussed. Fabricated devices exhibit small V_T variability and accumulation-mode like behaviors. The origins of these phenomena are discussed.

1. Introduction

One of the most critical issue of poly-Si NW transistors is the difficulty of achieving sufficient small variability characteristics. High density trapping states at grain boundaries (GBs) undermine not only carrier transports but also variability particularly in small-size NW transistors due to randomness of GBs placements [1]. Meanwhile, the concept of a junctionless (JL) NW transistor has been spotlighted due to its simple process and unique volume conduction [2]. High channel concentration usually produces severe V_T fluctuations induced by random dopant fluctuation (RDF) and width variation, which rapidly increases as the transistor is scaled down [3, 4]. However, there are only a few reports on the variability issues of the GAA poly-Si JL NW transistors.

In our previous work [5], we implemented the high performance GAA poly-Si JL NW transistor with ideal subthreshold slope (60.08 mV/dec) by improved quality of poly-Si from B segregation and F passivation effects. In this study, V_T variability ($\sigma V_T/T_{ox}$) and corner effects are highlighted.

2. Experimental

The device fabrication basically follows Ref. [5] (Fig.1a). BF_2^+ ions were implanted on the 120nm-thick SPC poly-Si film to form the p^+ channel. Then, active region was locally thinned down by thermal oxidation, where B concentration of thinned region was reduced due to the segregation, resulting in $P^+/P/P^+$ structure with low channel concentration in a self-align manner (Fig.1b). The NW/NS channel was defined by E-beam lithography and RIE, and suspended from the BOX layer by HF wet-etching. Then, 7nm gate oxide (T_{ox}) and 150nm in-situ doped N^+poly-Si were formed. After that, passivation, H_2 annealing, and Al metallization were carried out. The NW/NS length (L) and height (H) are 250 and 7nm, respectively. The NW width (W) ranges from 10 to 25nm and NS width from 55 to 130nm. The effective width (W_{eff}) is a perimeter, ranging from 34 to 274nm.

3. Results and discussion

Fig.2 shows the I_D-V_G curves of NW (W=10nm, W_{eff}= 34nm) and NS (W=130nm, W_{eff}=274nm) transistors at fixed L of 250nm (# of transistors = 40~50). Substrate bias of -25V was applied to eliminate the parasitic effects [5]. It is clearly seen that the variability becomes worse as W_{eff} decreases, which is attributed to the increased randomness of GBs placement and RDF.

Fig.3 displays the Pelgrom plot (σV_T-$(LW)^{-1/2}$) in comparison with previous reported poly-Si and bulk MOSFET. To remove the effect of T_{ox}, σV_T is divided by T_{ox}. Table I summarizes key parameters affecting σV_T of Ref. [6-9]. The clear linearity of $\sigma V_T/T_{ox}$ as a function of W_{eff} is observed. It is found that our results shows much smaller σV_T than JL transistors in [6] and comparable with poly-Si inversion-mode [7] and bulk transistors [9]. This is because better quality of poly-Si by F effect and low channel concentration by the B segregation. The small variability is a great advantage of our JL device.

It is known that JL transistors have a small corner effect due to volume conduction [10]. Fig.4a shows the average I_D values as a function of W_{eff} at gate-overdrive voltage (V_{ov}) of -2V, showing that I_D does not linearly increase as the W_{eff} increases. In addition, the I_D/W_{eff} decreases despite W_{eff} increases as shown in Fig.4b. One of possible reasons of this non-linearity is the corner effect by high electric field at the corner of NW even in the JL transistor. Fig.5 shows I_{D_total} as a function of $W_{NW}\times H_{NW}$ at different V_{ov}. When the $W_{NW}\times H_{NW}$ approaches to zero, I_D also approaches to zero at Vov=-0.1V (near the flat band condition) while I_D remains at Vov=-3V. This is because holes are accumulated at the corner due to high electric field at Vov=-3V (corner effect).

Following the component separation method [11], the ratio of the I_{D_corner} component is derived (Fig.6). Apparently, the narrower NW has larger fraction of I_{D_corner}, and it drastically decreases as V_G approaches to V_T due to the volume conduction of JL. This behavior is different from conventional JL transistor with high channel concentration. In our devices, the channel has low concentration and V_T is close to V_{FB}, resulting in accumulation-mode (AM) like behaviors [12] rather than normal JL operation. This is also a merit of our device because the current is higher even in narrow NW structure.

4. Conclusions

V_T variability and corner effect of GAA p-type poly-Si JL NW/NS transistors were experimentally examined. Small σV_T was obtained even in JL transistors thanks to high quality of poly-Si with low channel concentration. In addition, it was observed that our JL transistors have the large corner effect and show AM like behavior due to low channel concentration.

References [1] C. H. Ho *et al.*, IEEE TED, **59** (2012) 2396. [2] J. P. Colinge *et al.*, Nat. Nanotechnol., **5** (2010) 225. [3] A. Gnudi *et al.*, IEEE EDL, **33** (2012) 336. [4] G. Leung *et al.*, IEEE EDL, **32** (2011) 1489. [5] M. J. Ahn *et al.*, JJAP, **59** (2020) 070908. [6] H. B. Chen *et al.*, IEEE EDL, **34** (2013) 897. [7] M. Saitoh *et al.*, VLSI Symp. (2014) 178. [8] K. H. Jang *et al.*, IEEE SNW (2012) 59. [9] T. Mizutani *et al.*, SNW (2015) 21. [10] B. H. Lee *et al.*, Nano letters, **16** (2016) 1840. [11] K. H. Jang *et al.*, JJAP, **59** (2020) 021004. [12] J. P. Colinge *et al.*, *Semiconductor-on-Insulator Materials for Nanoelectronics Applications* (2011) 187.

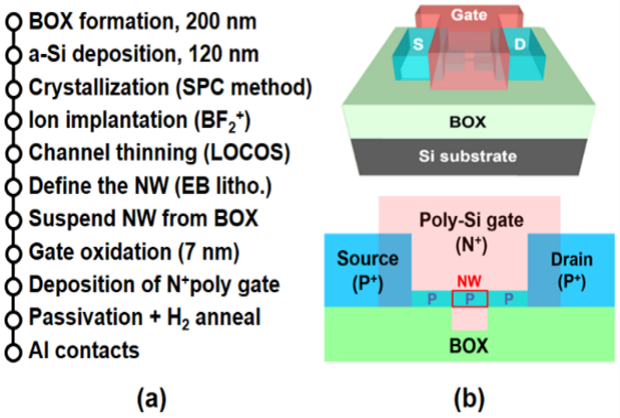

Fig.1: (a) Key fabrication process flows of GAA poly-Si JL NW/NS transistors, (b) 3D schematic and cross-section.

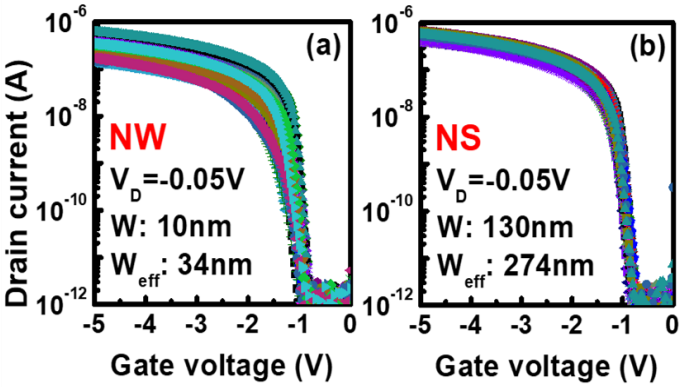

Fig.2: I_D-V_G curves of (a) NW (W=10nm, W_{eff}= 34nm) and (b) NS (W=130nm, W_{eff}=274nm) transistors with L of 250nm at V_{sub} of -25 V. 40~50 transistors were evaluated.

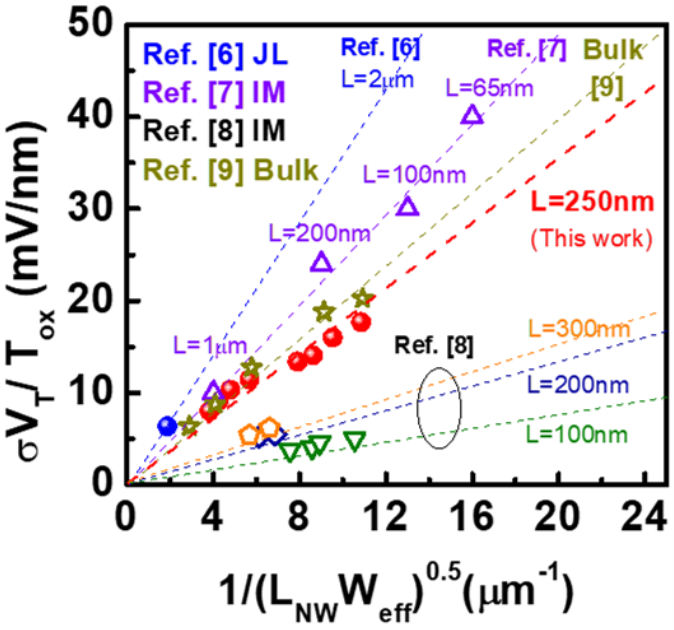

Fig.3: Pelgrom plot of σV_T. To remove the effect of T_{ox}, σV_T is divided by T_{ox} (y-axis: $\sigma V_T/T_{ox}$). Previous published data of poly-Si JL transistor [6], IM transistor [7, 8], and Bulk MOSFET [9] are also shown.

Table I: key parameters affecting the σV_T. Published poly-Si based NW IM, JL transistors, and Bulk MOSFET are compared.

	This study	Ref [6] JL	Ref [7] IM	Ref [8] IM	Ref [9] Bulk
W_{eff} [μm]	0.034 to 0.274	0.144	0.05 to 0.08	0.024	0.14 to 2
L_{NW} [μm]	0.25	2	0.1 to 0.3	0.065 to 1	0.06
T_{ox} [nm]	7	13	8	2	2
N_{ch} [cm^{-3}]	~1x10^{18}	~ 5x10^{18}	~1x10^{15}	~1x10^{15}	~1x10^{18}

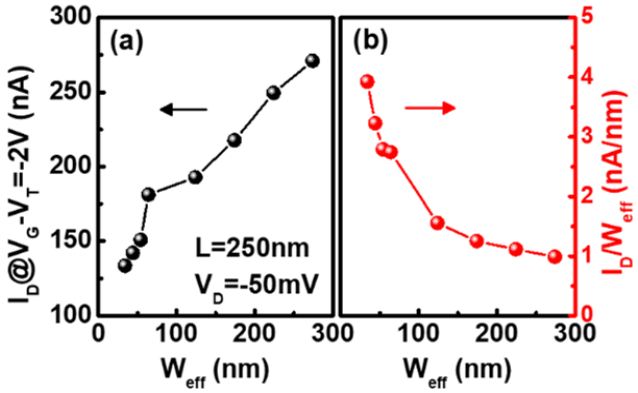

Fig.4: Extracted average (a) I_D and (b) I_D/W_{eff} as a function of W_{eff} with L of 250nm at gate-overdrive voltage (V_{ov}) of -2V.

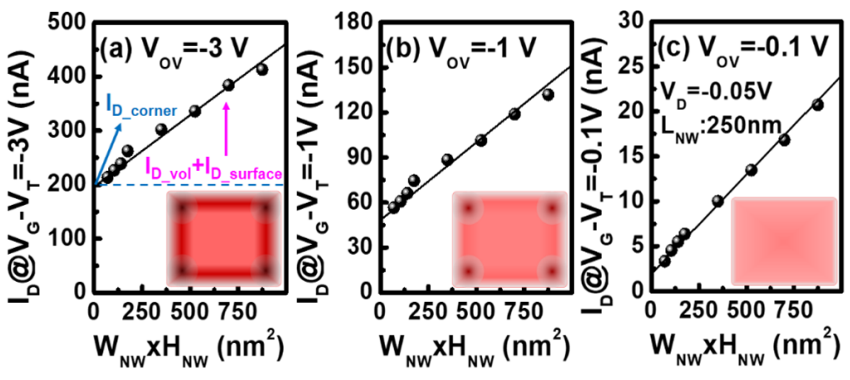

Fig.5: Extracted average I_{D_total} as a function of W_{NW}×H_{NW} at different V_{ov} of (a) -3 V (far from V_T), (b) -1 V, and (c) -0.1 V (close to V_T). The inset shows a schematic of NW cross-section showing the carrier density distribution.

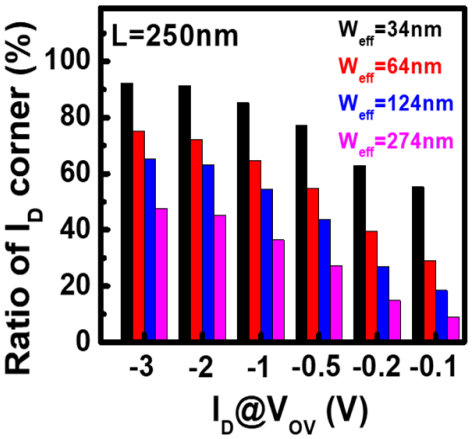

Fig.6: Ratio of I_{D_corner} of I_{D_total} with different W_{eff} as a function of various V_{OV}.