

Fermi-level Depinning of Metal-n-Ge by Carbon Nanotube Film Insertion

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Abstract

Ge CMOS has been recognized as one of the most promising next-generation technologies for extending Moore's law, since the high carrier mobility and Si-compatible process of Ge. However, one of the critical issues urgent to be solved is the Fermi-level pinning (FLP) of metal-n-Ge which seriously degrades performance of Ge MOSFETs. Insulator-insertion is one main technique for FLP modulation of metal-n-Ge, however, the performance is still not satisfying and the mechanism is controversial either. Here, we propose a new technique of carbon nanotube (CNT) film insertion, where the inserted film is a conductive layer instead of an insulator. Fermi-level depinning is realized, and is explained by a novel composite mechanism considering the metal induced gap states (MIGS) effects of both metal and CNTs, supporting the MIGS mechanism for FLP.

1. Introduction

As the Si CMOS technology approaches its physical limit, Ge CMOS is recognized as a promising next-generation technology for continuing the Moore's law, i.e. more Moore, not only because Ge has an obvious mobility advantage over Si but also thanks to its compatible process with Si [1]. However, one of the critical issues for Ge CMOS is the relatively large contact resistance of metal-n-Ge. The contact resistivity is exponentially dependent on $\phi N^{-0.5}$ where ϕ is the Schottky barrier height and N is the doping concentration of Ge. Since Ge has an issue of relatively low impurity solubility, a metal selection for a small ϕ is highly needed. However, generally for metal-n-Ge, the Fermi-level of Ge at the interface is almost perfectly pinned near the valence band edge, making metal selection meaningless. It is essential to alleviate the FLP for a small contact resistance of metal-n-Ge [2].

One main strategy for FLP modulation of metal-n-Ge is ultra-thin insulator insertion between metal and n-Ge [3-11]. Nishimura et al. modulated the FLP by insertion of a ~2-nm-thick GeO₂, however the on-current was weakened since the tunneling resistance [3]. Baek et al. inserted graphene layer between metal and n⁺-Ge leading to modulation of FLP, however, the pinning was not fully released for the thin thickness of graphene [4]. Besides the performance not satisfying, the

mechanism is still under debate. The alleviation of FLP may be due to MIGS effect reduction as well as interfacial state passivation by the insulator.

Here, we demonstrate Fermi-level depinning of metal-n-Ge by CNT film insertion. This conductive layer insertion leads to obvious Fermi-level depinning, and is explained by a composite mechanism considering the MIGS effects of both metal and CNTs, supporting the MIGS mechanism for FLP.

2. Results

Device Fabrications

The metal-CNT film-Ge junction was fabricated by transferring a CNT film onto a Ge substrate followed by metallization (Fig. 1). An n-Ge wafer (~ 0.3 Ω cm) was used as a substrate. After cleaning, an Ohmic Ti/Au bottom electrode was formed by scratching the substrate. CNT films were collected by the floating catalyst chemical vapor deposition (FCCVD) method (Fig. 2) [12]. By adjusting the deposition time at a constant rate of CNT collection, the CNT films with different thickness were obtained on filters. A CNT film was transferred one or several times by pressing the filter onto the substrate, followed by wetting with IPA droplets. By using CNT films with different deposition time and transfer times, CNT films with different thickness and density were inserted for devices D1-D6 (Table 1). Top electrode metallization (Au/Ti/Al) was made by the standard photolithography. Finally, the CNT film outside the electrode was etched by O-plasma, leading to an array of metal-CNT-n-Ge junctions (Fig. 3).

Electrical Characteristics

With the top electrode grounded, 20 IV characteristics for each of devices D1-D6 demonstrate a good uniformity of the junctions, with a clear variation of leakage current which is due to the FLP modulation and changing of the Schottky barrier height (Fig. 4). Using the histogram, the leakage current is analyzed statistically showing that with the increase of CNT thickness and density, the leakage current first increases and then decreases, with a peak value achieved by D4 (Fig. 5a). This is more obvious when typical IVs are compared directly (Fig. 5b). The symmetrical IV characteristics of D4 indicates an obvious Fermi-level depinning.

With the increase of CNT film thickness from D1 to D4, MIGS effect of metal is reduced leading to FLP modulation and increased leakage current. However, when the thickness and density of the CNT film further increase from D4 to D6, the increased electron density of the CNT film will generate MIGS effect again, leading to the decrease of leakage current. This novel composite mechanism gives a support to the MIGS mechanism for FLP.

3. Conclusions

Fermi-level depinning of metal-n-Ge by insertion of CNT films has been demonstrated. A composite mechanism considering MIGS effects of both metal and CNTs is proposed to explain the junction behavior, which supports the MIGS mechanism for FLP.

Acknowledgements

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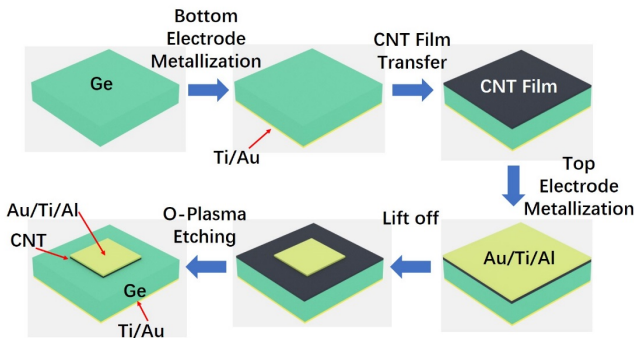


Fig. 1 Schematic diagram of device fabrications.

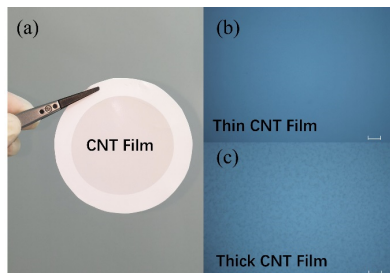


Fig. 2 Optical images of CNT films with different thickness made by the FCCVD method (scale bar: 10 μm).

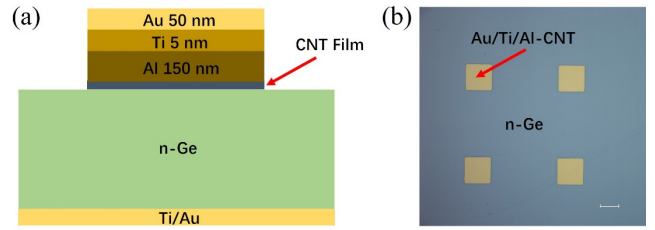


Fig. 3 Illustration and optical images of the device structure (scale bar: 50 μm).

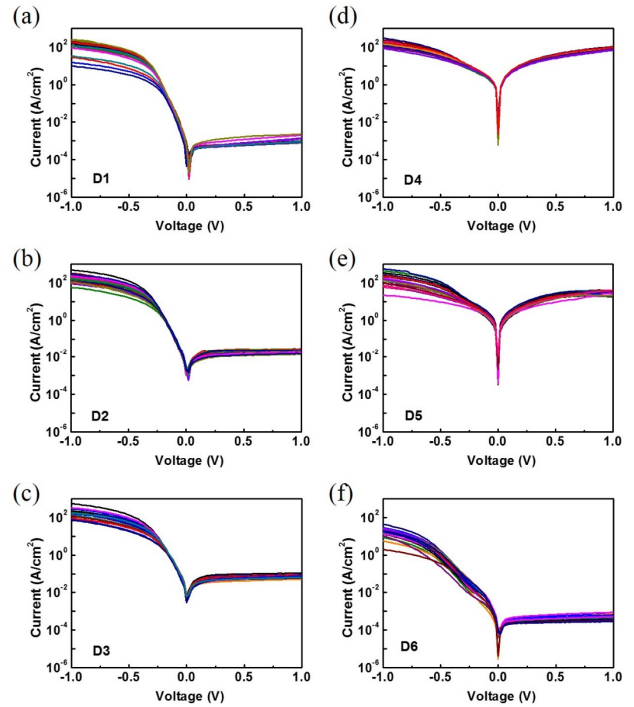


Fig. 4 IV characteristics of metal-CNT-n-Ge junctions with different CNT thickness and density. 20 IVs are shown for each case.

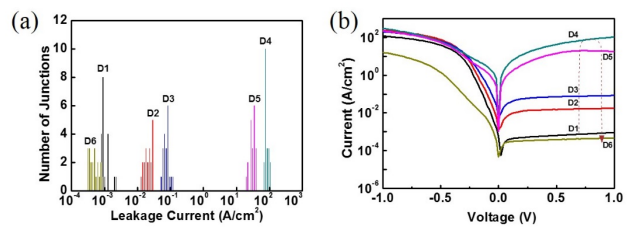


Fig. 5 Analysis of IV characteristics of metal-CNT-n-Ge junctions with different CNT thickness and density.

Table I CNT films

| CNT Film Device | Deposition Time (s) | Transfer Times |
|--------------------|---------------------|----------------|
| D1 | w/o CNT | w/o CNT |
| D2 | 10 | 2 |
| D3 | 10 | 4 |
| D4 | 180 | 1 |
| D5 | 360 | 1 |
| D6 | 720 | 1 |