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ON current enhancement and single-electron transport in tunnel FETs by a new isoelectronic trap impurity of beryllium

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Abstract

We have experimentally demonstrated ON current enhancement and single-electron transport in tunnel FETs (TFETs) by introducing a new isoelectronic trap (IET), beryllium. In previous studies, we showed that the introduction of the Al-N complex IET impurity enables an ON current enhancement as a conventional transistor and high-temperature operation as a qubit, making the TFETs more functional. The Be IET, proposed newly this time, also enhances the ON current of the TEFT by 5 times. Moreover, as a single-electron transistor, the charging energy of 0.4 eV has been obtained. This suggests that Be IETs can be used as more temperature-stable quantum bits. Thus, the functionalization of TFETs also can be realized by Be IET.

1. Introduction

Tunnel FETs (TFETs) are one of the candidates for steep switching devices to realize low operation voltage CMOS circuits. Silicon TFETs is difficult to improve the ON current due to the low indirect inter-band tunneling probability. Mori *et al*. proposed the introduction of an isoelectronic trap (IET) to provide pseudo-direct tunneling (Fig. 1(a)) in order to increase the tunneling probability [1,2]. By introducing Al-N IET, they experimentally demonstrated the ON current enhancement of TFETs [1].

Moreover, the IET functionalizes the TFETs as quantum bits (qubits). The present operation of Si qubits has been restricted to milli-Kelvin temperatures, thus limiting the application. The qubit utilizing IET-TFET act as an electron spin qubit and can be operated at high temperatures up to 10 K, that is the record highest temperature for the operation of silicon spin qubits [3]. If the high-temperature operation of Si qubits is realized, the range of applications could be extended.

This study proposes Be as a novel IET impurity to functionalize TFET as stated above. Be IET is known to form deeper energy levels than Al-N IET [4]. We experimentally show that it is able to achieve ON current enhancement and single-electron operation of TFETs, by introducing Be IET into the channel of Si-TFETs.

2. Experiment

Fig. 1(b) shows the device fabrication process, which is almost the same as that in the previous report [5]. We utilized SiO_2/HfO_2 (1.0 / 4.0 nm) films as a gate insulator and a TaN film as a metal gate. The post-implantation annealing (PIA) conditions after Be ion implantation (I/I) were the same as for Al-N at 450°C for 24 hours.

3. Results and Discussion

Starting with the Be IET formation process. Photoluminescence (PL) spectra from Be and Al–N implanted Si samples and secondary-ion mass spectroscopy (SIMS) profiles of Be with different PIA conditions are shown in Fig. 2. Here, the Be I/I energy and dose are 15 keV and 5×10^{13}cm^{-2}, respectively. As shown in Fig. 2(a), a sharp Be-Be emission line was observed at 1.079 eV as reported in the previous work [4]; therefore, the formation of Be IET in the Si band gap was confirmed. The Be-Be emission line has lower energy than the Al-N emission line, indicating the formation of deeper impurity levels in the Si band gap. In Fig. 2(b), the Be concentration with PIA at 450°C for 24 h was largely reduced than that at 450 °C for 30 min. In contrast,

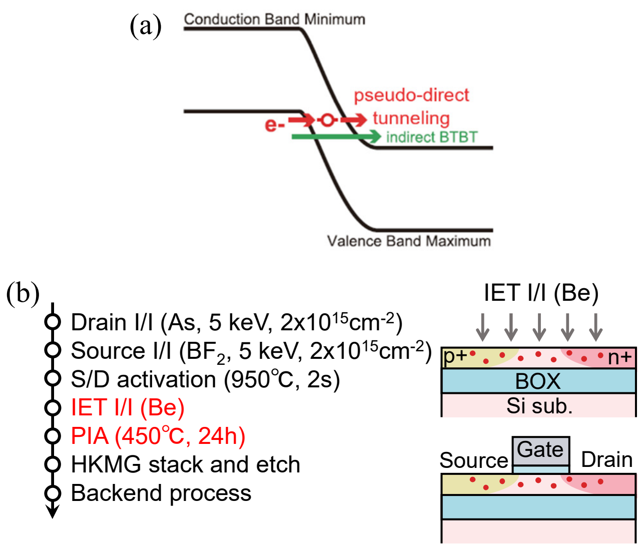

Fig. 1 (a) Schematic of the band diagram of tunneling transport through PN junction. IET intermediated and conventional tunneling paths (indirect BTBT) are illustrated. (b) Process flow and schematic cross-sections of the device fabrication method.

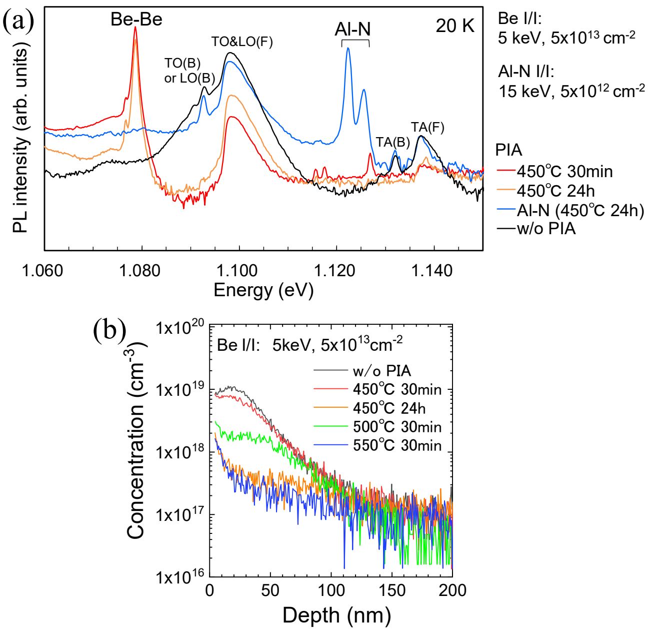

Fig. 2. (a) PL spectra of the energy. Be-Be isoelectronic emission peaks at different PIA times are shown. (b) Impurity depth profiles measured by SIMS for Be.

as shown in Fig. 2(a), the PL intensity of Be-Be does not decrease much at 450 °C for 24 h compared to 450 °C for 30 min. This indicates that Be desorption by PIA is not a problem for Be-IET level formation. Furthermore, emissions originated from defects observed in the PL spectra at 450°C for 30 min are reduced at 450°C for 24 h (not shown). This is due to the recovery of the defects in Si samples. Hence, the PIA after Be I/I at 450 °C for 24 h was employed for the investigation of the transport in the channel of TFETs through the Be level.

Fig. 3 presents the I_D –V_G characteristics and the variation statistics of ON current (I_{ON}) for the TFETs (L_g = 3μm, W_g = 5 μm) with Be I/I at room temperature. The ON current of the Be-IET-assisted N-TFETs is about 5 times higher than that of the control fabricated in the same process, which is larger than that of the Al-N IET [5]. In addition, as shown in Fig. 3(b), Be I/I improves the variability of N-TFETs significantly as is the case of Al-N [6]. This result suggests that it is able to fabricate TFETs with operational stability and lower power consumption by introducing Be.

Fig. 4 shows the intensity map of the differential conductance dI_D/dV_S of Be implanted TFET (L_g = 80 nm, W_g = 1 μm) at low temperature (1.5 K). Clear Coulomb diamonds were observed in this map, that indicates the TFET operates as a single-electron transistor. The single electron charging energy estimated from the widths of these Coulomb diamonds are up to 0.4 eV. This energy value is about 15 times higher than room temperature, suggesting high temperature stability in in the use of Be IET as a qubit. Moreover, this value is larger than the charging energy of Al-N IET in TFETs, about 0.2 eV. This suggests the availability of Be IET for high-temperature operation of Si qubits.

4. Conclusions

We fabricated TFETs with a new Be IET and two functionalization was successfully demonstrated, ON current enhancement in conventional transistor operation and single-electron operation with a large charging energy. These indicate that utilizing Be IET in Si is promising to realize low power consumption TFETs and high-temperature operating qubits.

Acknowledgements

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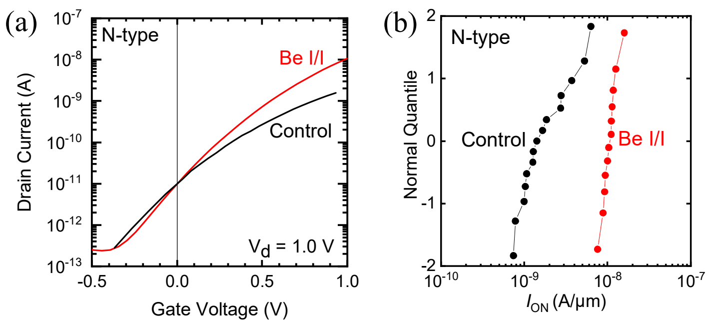

Fig. 3 (a) I_D–V_G curves of the control and Be implanted IET-TFETs. Their L_G and W_G were 3 μm and 5 μm, respectively. (b) Normal quantile plot of I_{ON}, which was extracted at the voltage of V_G –V_{TH} = 1.0 V with V_D = 1.0 V.

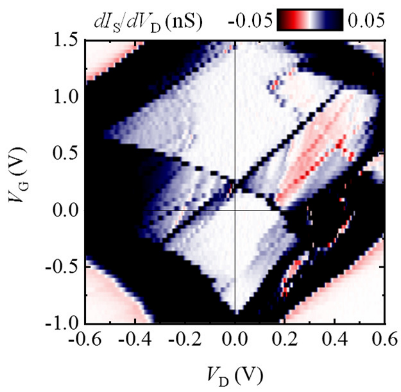

Fig. 4 Linear-scale dI_S/dV_D maps of a Be-implanted TFET (L_g = 80 nm, W_g = 1 μm) at low temperature (1.5 K).