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# A Self-Bias NAND Gate and its Application to Non-Overlapping Clock Generator for Extremely Low-Voltage CMOS LSIs

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**Abstract**

**This paper presents a self-bias NAND (SBNAND) gate and its application to a non-overlapping (NOL) clock generator for extremely low-voltage CMOS LSIs. The SBNAND consisting of a main NAND gate and feedback inverter improves the output performance at extremely low supply voltage $V_{DD}$ by controlling the body bias voltages $V_{BS}$ of the main NAND gate. Measurements of a proof-of-concept chip demonstrated that our proposed NOL clock generator using SBNANDs can operate at extremely low $V_{DD}$ of 60 mV.**

## 1. Introduction

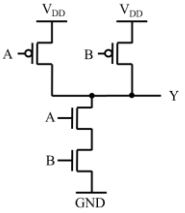
Extremely low-voltage (ELV) circuit design techniques are expected to expand next-generation emerging LSI applications. Several ELV design techniques have been studied [1]-[3]. Matsuzuka *et al.* reported an ELV ring oscillator (ROSC) consisting of self-bias inverters (SBINVs) [1]. The ROSC operated at an extremely low voltage of 42 mV. In order to utilize the low-voltage clock signals in peripheral circuits and to move to the next design step, we have to explore and develop fundamental logic gates.

In light of this background, we propose a self-bias NAND (SBNAND) as an ELV fundamental logic gate. The SBNAND consists of a main NAND gate and feedback inverter. The performance of the SBNAND is improved by controlling body bias voltages of the main NAND gate. We also develop a non-overlapping (NOL) clock generator using SBNANDs and SBINVs. Measurements of a proof-of-concept chip demonstrate that our proposed NOL clock generator can operate at extremely low supply voltage.

## 2. Proposed SBNAND

Figures 1(a) and 1(b) show a schematic and truth table of the NAND gate, respectively. As with the case in [1], the transfer characteristics of the NAND gate degrades as the supply voltage $V_{DD}$ decreases less than several 100s mV. The output voltage swing decreases significantly due to the leakage current of the MOS transistors.

To solve the problem, we consider modifying the NAND gate by controlling threshold voltages, $V_{THN}$ and $V_{THP}$, through the body bias voltages, $V_{BS}$. Figure 1(c) summarizes our proposed control scheme. When the output Y is to be high,




(a)

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b)

| Y | $V_{THN}$ | $V_{THP}$ | $V_B$ |
|---|---|---|---|
| 1 | High | Low | 0 |
| 1 | High | Low | 0 |
| 1 | High | Low | 0 |
| 0 | Low | High | 1 |

(c)

Fig. 1 (a) Schematic of the NAND gate, (b) its truth table, and (c) proposed control scheme.

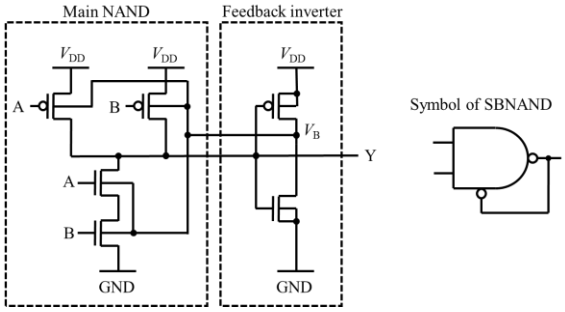



Fig. 2 Schematic of the proposed self-bias NAND gate and its circuit symbol.

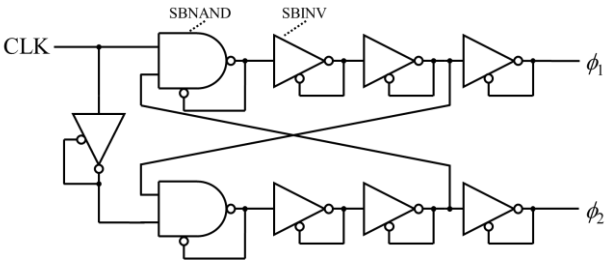



Fig. 3 Schematic of the non-overlapping (NOL) clock generator.

threshold voltages of nMOS and pMOS transistors in the NAND gate should be set to high and low, respectively, to keep the output Y high. On the other hand, when the output Y is to be low, threshold voltages of nMOS and pMOS transistors should be set to low and high, respectively, to keep the output Y low. To realize the threshold voltage conditions shown in Fig. 1(c), we can find that the inverting logic of Y can be used as a control voltage of $V_B$.

Figure 2 shows a schematic and symbol of our proposed self-bias NAND (SBNAND) gate. The SBNAND consists of a main NAND gate and feedback inverter. The output voltage of the feedback inverter is connected to the body of the main NAND gate and controls the threshold voltages $V_{TH}$s of the main NAND's transistors.

As an application circuit using the proposed SBNANDs, we develop a non-overlapping (NOL) clock generator circuit. Figure 3 shows a schematic of the NOL clock generator consisting of SBNANDs and SBINVs.

## 3. Experimental Results

We fabricated a proof-of-concept chip of our proposed NOL clock generator (Prop.) using a 0.18-µm, 1-poly, and 6-metal CMOS technology with deep n-well option. The conventional NOL clock generator (Conv.) was also fabricated in the same chip for comparison. Figure 4 shows a micrograph of our chip. The number of the delay cells in the NOL clock generator was set to 2, 4, 6 and 8. The areas of Prop. and Conv. using 2 delay cells were 2,805 and 152 µm$^2$, respectively. In the measurement, we used source followers to sufficiently drive off-chip parasitics (bias current was set to 10 µA).

Figure 5 shows the measured waveforms of (a) Conv. and (b) Prop. at $V_{DD}$ = 60 mV. The amplitudes of the conventional and proposed clock signals were 28.7 and 50.3 mV, respectively. Higher amplitude was obtained by using our proposed NOL clock generator as shown in Fig. 5(b).

Figure 6 shows the measured normalized amplitude as a function of $V_{DD}$. The proposed NOL clock generator could generate a stable clock at extremely low $V_{DD}$. We defined the minimum $V_{DD}$ as the voltage at which the normalized amplitude was higher than 0.8×$V_{DD}$. The minimum $V_{DD}$ of the proposed and conventional NOL clock generators were 60 and 70 mV, respectively.

## 4. Conclusions

In this work, we proposed a self-bias NAND (SBNAND) gate as an extremely low-voltage fundamental logic gate. The SBNAND consisting of a main NAND gate and feedback inverter improved the output voltage swing at extremely low voltage supply. Measurement results demonstrated that the non-overlapping clock generator using SBNANDs operated at extremely low supply voltage of 60 mV.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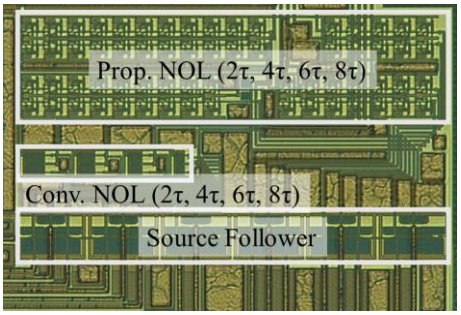


Fig. 4 Chip micrograph.

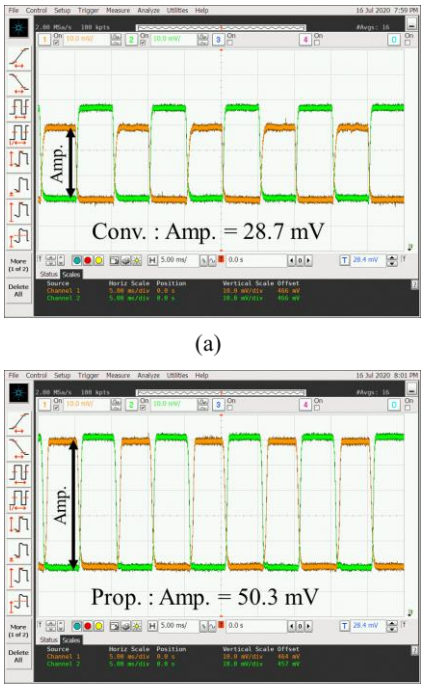


Fig. 5 Measured waveforms of (a) the conventional and (b) the proposed NOL clock generator at $V_{DD}$ = 60 mV.

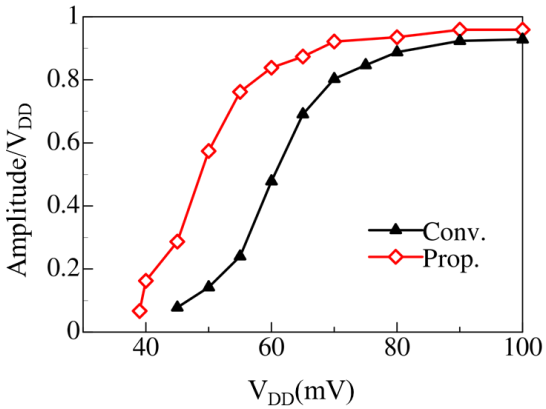


Fig. 6 Measured normalized amplitude of the NOL clock generator as a function of $V_{DD}$.


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