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Nonvolatile SRAMs Enabled by Hysteretic Negative-Capacitance FETs - A Comparative Study of Novel 9T and 8T nvSRAMs

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Abstract

This work conducts a comparative study of two nonvolatile SRAM cells enabled by hysteretic negative-capacitance FETs. With the aid of a short-channel 2D-NCFET SPICE model, the stability, performance and energy consumption of novel 9T and 8T nonvolatile SRAMs have been investigated and compared. Our study indicates that, as compared with the 8T counterpart, the 9T nvSRAM possesses better write stability and read performance at the expense of slightly larger energy consumption during write and restore operation due to the higher transistor count. Both the NCFET-based nvSRAMs exhibit superior energy-efficiency than other types of nvSRAMs, which is crucial to power-gating applications.

1. Introduction

Compact embedded nonvolatile memories with fast data access ability is crucial for energy-harvesting near-memory computing. Several nonvolatile SRAM solutions with additional circuitry or nonvolatile memories (e.g., RRAM, MTJ, etc.) for data backup and restore have been proposed in the literatures [1]-[4]. However, the unsatisfactory power off-on energy ($E_{S\&R}$) due to high static current in existing nvSRAMs prohibits the energy savings. In [5], a 6T2C nvSRAM cell with two ferroelectric capacitors connected to a standard 6T SRAM cell has been demonstrated experimentally. Nonetheless, the area penalty due to ferroelectric capacitors remains the major drawback compared with using transistors. Thanks to the recent discovery of ferroelectricity in doped hafnium-oxide [6], the negative-capacitance FET (NCFET) [7] with steep SS and improved on-state current has garnered substantial interest. Depending on the capacitance matching, the hysteretic-NCFET in I_D-V_G characteristics can also be seen. In this work, the stability, performance and energy consumption of novel 9T and 8T hybrid nvSRAMs employing 2D-FETs and hysteretic 2D-NCFETs are comprehensively examined and compared.

The schematics of the hybrid nonvolatile 9T and 8T SRAM cells are shown in **Fig. 1(a)** and **Fig. 1(b)**, respectively. 2D-FETs with their atomically-thin thickness has the potential for future high-density 3D technology [9]. Monolithic-3D integration offers the possibility to independently optimize two different technologies [10] such that the nonvolatile circuitry of the hybrid nvSRAM cells can be realized in the NCFET-tier as illustrated in **Fig. 2**.

2. Methodology

To evaluate the stability and performance of the hybrid nvSRAM cells, an accurate and physical short-channel 2D-NCFET compact model [11] calibrated with TCAD numerical simulation is adopted as shown in **Fig. 3 (a)**. The hysteretic NCFET is simulated by coupling the surface-potential-based model of the underlying 2D-FET with the 1D Landau-Khalatnikov (LK) equation in the SPICE simulator. The ferroelectric parameters of HfZrO used in this work ($\alpha = -3.8\times10^9$ m/F, $\beta = 3.37\times10^{11}$ m^5/F/C^2, $\gamma = 0$ m^9/F/C^4) are extracted from the published data [12]. Pertinent parameters of channel materials (monolayer MoS_2 and WSe_2) are judiciously chosen from the published literature [11]. The hysteretic 2D-NCFET in the hybrid nvSRAM cells can possess two states in the hysteresis loop around V_{gs} = 0V by design as shown in **Fig. 3(b)**. One state can switch to the other with a sufficiently positive or negative gate-to-source voltage.

3. Results and Discussion

Fig. 4 shows the transient waveforms and the operation concept of the 9T nvSRAM during restoration. For normal SRAM operation, the restore signal is grounded which isolates the nonvolatile circuitry from the storage node. The grounded restore signal also turns on the additional PMOS (MP1) and passes the value of V_R to the source terminal of the hysteretic-NCFET. During the recall period, the restore signal needs to be raised to V_{DD} in advance. The final state of the V_R will depend on the polarization state of the hysteretic-NCFET as shown in **Fig. 4**. Note that the additional NMOS (MN1) is stronger than the pull-up PMOS due to the NC-effect so that the storage node can be successfully pulled-down to ground. The three-transistor restore circuitry has also been used to realize nonvolatile flip-flop in [13].

Butterfly curves for the read and write operation at (a) V_{DD} = 0.7V and (b) V_{DD} = 0.5V are demonstrated in **Fig. 5**. Since the restore signal is grounded during normal SRAM-mode, the extra circuitry of the 9T nvSRAM does not affect its read/write operation and stability. **Fig. 6** shows the comparison of the RSNM and WSNM at V_{DD} = 0.7V and 0.5V, respectively. Note that the 9T nvSRAM shows nearly identical results with the baseline 6T SRAM. However, the previously reported 8T nvSRAM exhibits improved RSNM but degraded WSNM. This is because the hysteretic-NCFETs are in series with the pass-gates (PGs) of the baseline 6T SRAM serving as extra resistors weakening the PGs during read and write operation. With a lower supply voltage (**Fig. 6(b)**), the weakening effect can be alleviated due to the increasing ON-state current ratio of the hysteretic-NCFET and the baseline 2D-FET.

The performance comparison including read access time and time-to-write are shown in **Fig. 7.** Larger read access time of the 8T nvSRAM results from the degraded read current. **Fig. 8** shows the energy consumption during the read and write operation. Slightly larger write energy of the 9T nvSRAM can be attributed to the extra capacitance from the restore circuitry. **Fig. 9** illustrates the benchmarking of the power off-on energy ($E_{S\&R}$) and break-even-time (BET) time for several different nvSRAMs reported [1]-[4]. It is clear that, compared with the RRAM and MTJ based nvSRAMs, the NCFET-based nvSRAMs exhibit superior energy-efficiency which is favorable for power-gating applications. **Fig. 10** shows the overall comparison of the NCFET-based 9T and 8T nonvolatile SRAM cells. Although the 9T nvSRAM demonstrates better write stability and read performance, the energy consumption during write and restore operation is slightly larger due to the higher transistor count.

Acknowledgements

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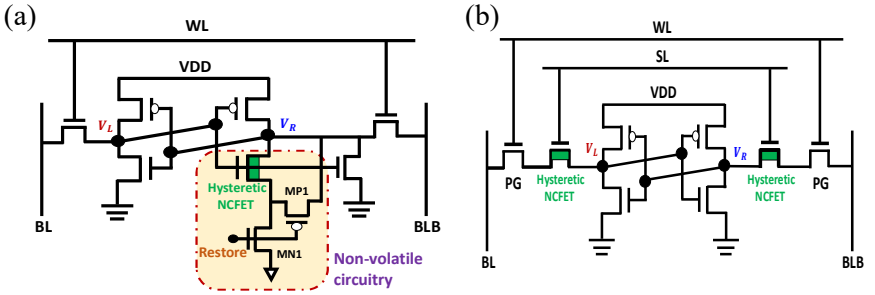

Fig. 1. (a) Schematic of the 9T nonvolatile SRAM cell. Three extra transistors including a hysteretic-NCFET and two hysteresis-free NCFETs are used for data restore operation. **(b)** Schematic of the previously reported 8T nonvolatile SRAM cell [8]. Two hysteretic-NCFETs are inserted in series with the PGs of the traditional 6T SRAM for data restoration.

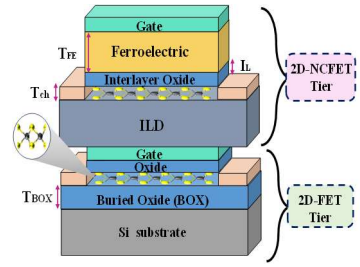

Fig. 2. Schematic illustration of the two-tier monolithic 3D stacking. Depending on the upper-tier interlayer oxide thickness, the NCFET can be hysteresis-free or hysteretic.

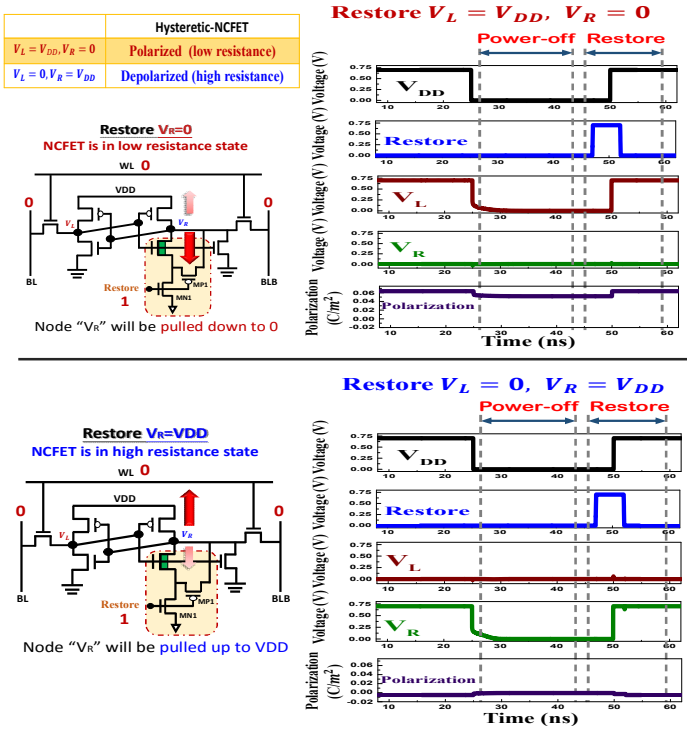

Fig. 4. The transient waveforms of the 9T nvSRAM during backup/restore operation. Note that the polarization state of the hysteretic-NCFET may vary and backup automatically along with the storage nodes.

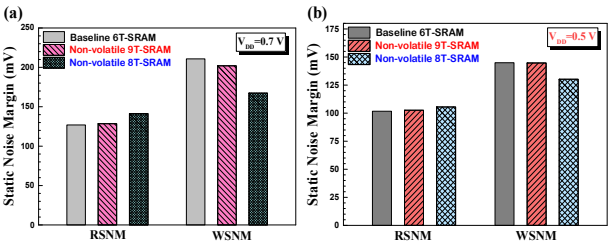

Fig. 6. Comparison of the RSNM and WSNM at **(a)** V_{DD} = 0.7V and **(b)** V_{DD} = 0.5V. The 9T nvSRAM shows nearly identical results with the baseline 6T SRAM.

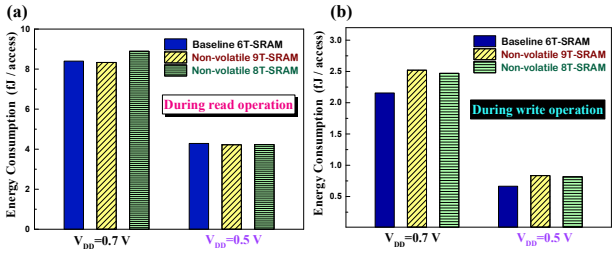

Fig. 8. Comparison of the energy consumption during **(a)** read operation and **(b)** write operation at V_{DD} = 0.7V and 0.5V. Slightly larger write energy of the 9T nvSRAM is attributed to the extra capacitance from the restore circuitry.

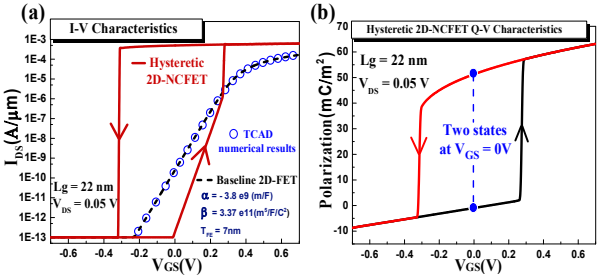

Fig. 3. (a) I_{ds}-V_{gs} and (b) P-V_{gs} characteristics of the hysteretic-NCFET simulated in this work. Two states straddling V_{gs}=0 can be seen.

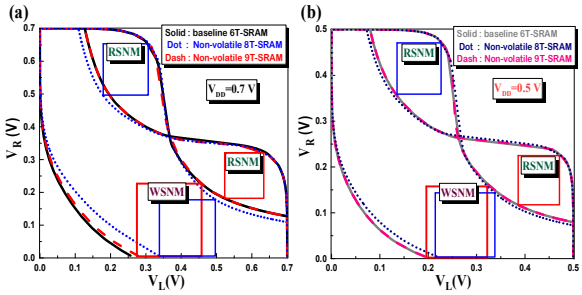

Fig. 5. Butterfly curves for the read and write operation at **(a)** V_{DD} = 0.7V and **(b)** V_{DD} = 0.5V of the baseline 6T SRAM, the 8T nvSRAM and the 9T nvSRAM.

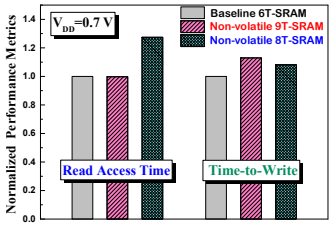

Fig. 7. Comparison of the read/write performance at V_{DD} = 0.7V. The capacitive load is estimated for the actual layout of 64 cells per bit line.

Compared with 6T-SRAM	Nonvolatile 8T-SRAM	Nonvolatile 9T-SRAM
RSNM	↑	→
WSNM	↓	→
Read access time	↑	→
Time-to-write	↑	↑
Read energy	↑	→
Write energy	↑	↑
Area overhead	↑	↑

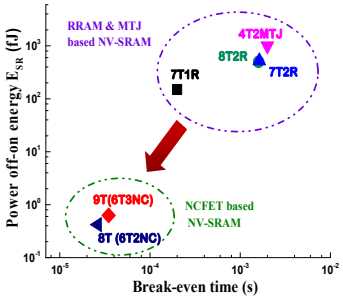

Fig. 9. Benchmarking of the power off-on energy and break-even time for several nvSRAMs in the literatures [1]-[4]. The power supply ramp-up time is assumed to be 1us for the 9T and 8T nvSRAMs.

Fig. 10. Comparison of the NCFET-based 9T and 8T nonvolatile SRAMs. The direction and length of the arrows indicate the increase/decrease of the value compared with the baseline 6T-SRAM.