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A Triple-Deck CFET Structure with an Integrated SRAM Cell for the 2nm Technology Node and Beyond

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Abstract

A novel triple-deck CFET structure is proposed for the first time as a candidate for area scaling. The proposed triple-deck CFET aggressively stacks a pass gate over an inverter to form a half SRAM bit cell. The integration flow and full metal connectivity have been carefully designed for functionality and array assembly. Most of the pitch used in the process is around 40nm, which is patternable using 193i litho process to reduce patterning cost and difficulty. We have also studied parasitic capacitance and resistance to evaluate design weakness of the proposed structure.

Introduction

Double-deck CFETs uses a common gate architecture of PFETs and NFETs stacked within an inverter[1, 2]. A triple-deck CFET makes full use of the symmetric properties of a standard 6T SRAM cell. Each triple-deck individual cell consists of a pull-down NFET, pull-up PFET and pass-gate NFET vertically stacked. As shown in Fig.1, this design uses 2 device footprints per bitcell, which provides a 50% area reduction from the 2-deck version [1]. The integration flow for a triple-deck CFET can also improve density for non-CMOS circuits that contain extra transistors, as well as SRAM cell architectures. In this study, we have modeled the process flow for a triple-deck CFET with a reduced EUV patterning scheme via Coventor's SEMulator3D® virtual fabrication platform[3].

Simulation Setup

A triple-deck CFET structure includes a pass gate stacked on top of a pull down and pull up transistor. The triple-deck CFET architecture requires a trade-off between area and integration complexity. A larger metal gate pitch may be required for the BEOL interconnects, as shown in Figures 1 and 2. In our design, we have set the CPP and Fin pitch at 60nm and 40nm respectively, to ensure a robust process flow. Our resulting SRAM cell area was 120nmX40nm (0.0048um^2), and Vdd and Vss run inside the buried metal rails. The wordlines (WL) and bitlines (BL) run orthogonally in metal lines a0.bove the buried metal rails, allowing row WL and column BL sharing.

Key Process Description

Source drain (S/D) epi is done sequentially, layer-by-layer from the bottom, with metal connections to the buried rails deposited as shown in Fig. 4. The lower channel S/D is covered by ODL (a), followed by a dummy spacer to protect the upper channel (b). Good etch selectivity between the dummy spacer and the actual spacer is required. Lower channel epi is complete after removal of the ODL and dummy spacer, and then the structure is covered by a dielectric. An S/D cut and nitride fill/CMP are required to guarantee good insulation of different regions of the device (see green nitride, Fig. 5). The bit line metal and via used by the shared node are filled prior to the replacement metal gate process. This step can be self-aligned at the source drain cut and dummy gate for easy overlay control. The RMG process is different from that of a traditional GAA-CFET technology, since the inverter gate will be separated from the PG transistor gate in Fig.6. Hence, metal fill should be etched back in order to fill the dielectric between the PG and PU channel. This step requires precise etch control over a limited region. Some advanced etch approaches, such as atomic layer etch, may be adopted to obtain the nanometer etch control required by this step.

Challenge of the Process

The internal node connection is a challenging task. The common source/drain of the PD/PU/PG are connected by a single metal pattern, which is subsequently connected to the gate on the opposite side using an upper metal structure. The pattern used is shown in Fig.7. During our modeling, we simulated parasitic resistance and capacitance for the structure to understand electrical performance. The highest current density location is found at the internal node connection to the opposing gate, as shown in Fig.8. This occurs due to the small dimension of the via. Gate connection resistance is only important when the cell is switched on during a write operation. Fig .9 displays the capacitance matrix of different metal nets. The internal node (Q/QB) is found to be a key location where we see large capacitance, due to its large proportional volume and overlap area with the WL. Patternability for all steps was evaluated to determine any requirements for EUV or other advanced lithography. Since the BL is self-aligned by the source drain cut between the transistors, a 120 nm pitch LELE process should be sufficient. Fig.3 lists most of the patterning minimum pitch requirements, which are designed to be large enough for 193i. The design of the fin pitch can be loosened to 40nm or even more to satisfy other requirements. Fig.10 shows that nanosheet GAAFET offers space for metal connections and separation cuts than nanowire GAAFET with the same effective width.

Conclusion

A triple-deck CFET structure and integration scheme have been proposed to provide up to a 50% increase in SRAM area scaling from a double-deck CFET structure. Full metal interconnectivity is planned for array implementation. Key enabling process steps of the flow are discussed in this paper, including careful consideration of reduced EUV lithography to minimizing patterning cost and difficulty. The internal node connection is the most challenging process step, along with the need for multiple dielectrics of strong etch selectivity between each other. This work also provides a path to implement vertical CFET structures outside of SRAM applications, into non-fully N/P symmetric circuits with extra transistors.

References

[1] J. Ryckaert *et al.*, *2018 IEEE Symposium on VLSI Technology*, 2018: IEEE, pp. 141-142.
[2] A. Mallik *et al.*, *2019 Symposium on VLSI Technology*, 2019: IEEE, pp. T202-T203.

[3] https://www.coventor.com/

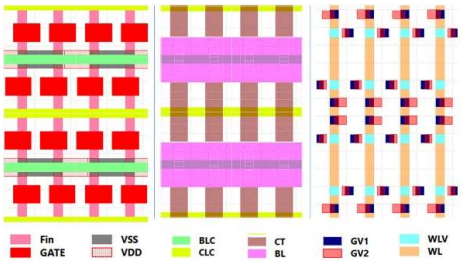

Fig.1 Layout design of CFET SRAMs

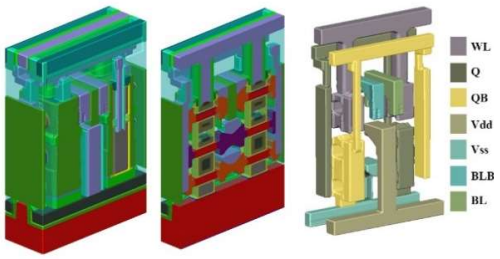

Fig.2 3D structure of triple-deck CFET SRAM and cutplane of channel，along with metal connections

Layer	min pitch	Patterning scheme
Fin	20 (logic), 40 (SRAM)	SAQP +LE2 (cut)
GT	60	SADP +LE2 (cut)
VDD	80	LE
VSS	80	LE
BLC	120	LE
CLC	120	LE
CT	40	LE2, SADP
BL	120	LE
GV1	30	EUV2/LE6
GV2	30	EUV2/LE6
WLV	40	SADP SAV/LE2 SAV/ EUV2
WL	40	SADP/LE2

Fig.3 Lithography assumption used in this work

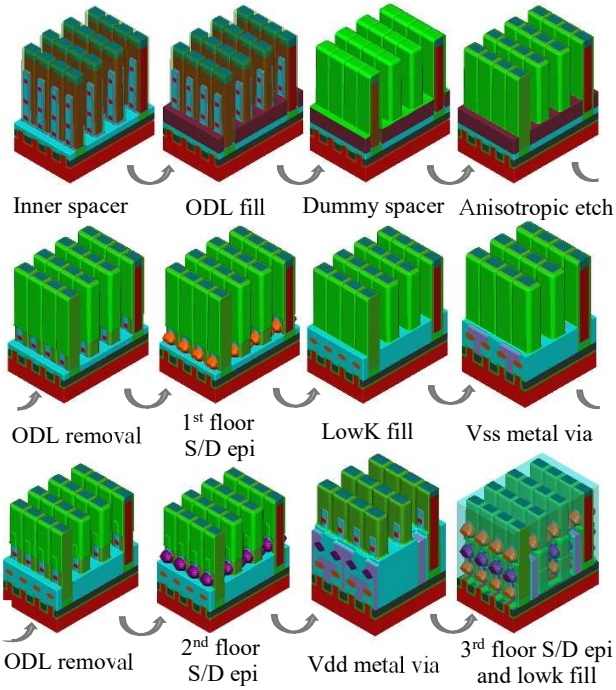

Fig.4 Process flow source drain schema with metal connections

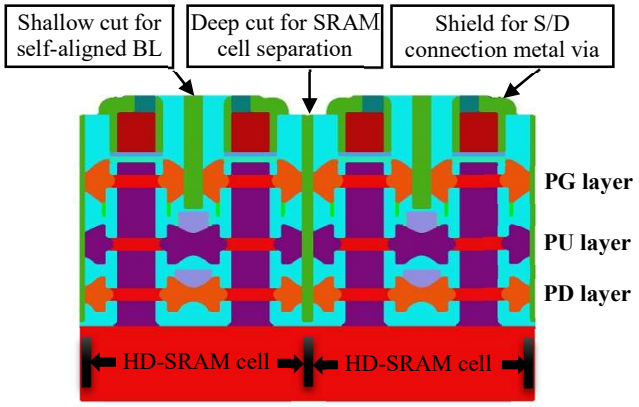

Fig.5 Cutplane on S/D cut with deep cut for internal node and shallow cut for bitline

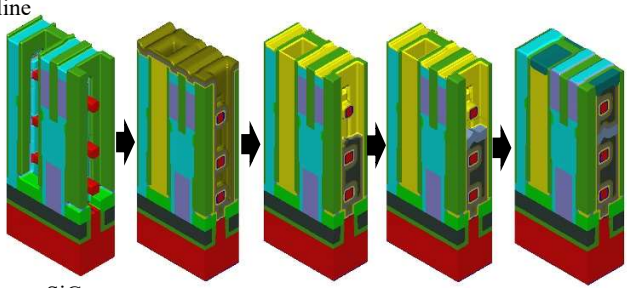

Fig.6 The process flow for the separation gate of pass gate transistor

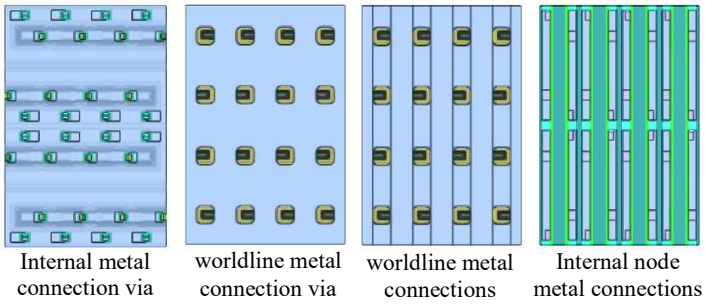

Fig.7 Metal connections for internal node and WL

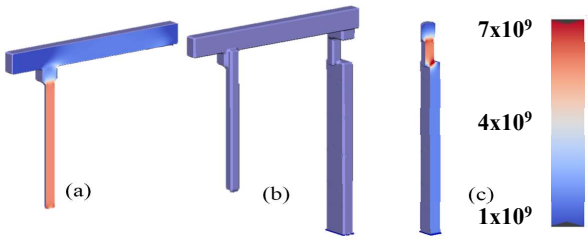

Fig.8 Current density with the internal connection in A/cm^2.

	WL	Q	QB	VDD	VSS	BLB	BL
WL		5.55E-05	5.56E-05	2.48E-06	2.17E-08	1.55E-05	1.40E-05
Q	5.55E-05		3.11E-05	8.26E-06	9.23E-06	4.81E-07	9.94E-07
QB	5.56E-05	3.11E-05		1.13E-05	8.56E-06	1.61E-06	3.72E-07
VDD	2.48E-06	8.26E-06	1.13E-05		1.43E-05	8.92E-07	8.79E-07
VSS	2.17E-08	9.23E-06	8.56E-06	1.43E-05		3.59E-09	2.79E-09
BLB	1.55E-05	4.81E-07	1.61E-06	8.92E-07	3.59E-09		9.11E-06
BL	1.40E-05	9.94E-07	3.72E-07	8.79E-07	2.79E-09	9.11E-06	

Fig.9 Capacitance matrix table between different nets in pF.

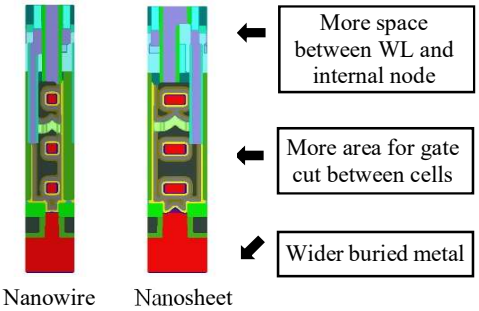

Fig.10 Comparison of nanosheet GAAFET and nanowire GAAFET