Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp105-106

Sidewall Erased Multiple-Time Programmable Memory Cells in FinFET Technologies

Chun-Yu Chuang, Chrong-Jung Lin, and Ya-Chin King
Microelectronics Laboratory, Institute of Electronics Engineering,
National Tsing Hua University, Hsinchu, Taiwan
Phone/Fax: +886-3-5162219, E-mail: ycking@ee.nthu.edu.tw

Abstract

A multiple-time programmable (MTP) memory cell with contact erase gate is proposed and implemented in a 16nm FinFET process. The new erase gate structure with a more compact cell enable electrons to tunnel through the sidewalls between metal gate and contacts. Independent erase gate biasing can be used to further enhance the read window in larger arrays. Good cycling reliability and disturb immunity are also demonstrated on the proposed cells.

Introduction

The rapid development of IoT applications generates increasing needs for high density embedded non-volatile memories (eNVM) [1]. Logic NVM solutions [2] have a main advantage over conventional eNVM approaches, its fully compatibility to CMOS logic processes, leading to reduced costs and increased integration flexibility. In a previous report [3], a single poly-silicon floating gate MTP cell based on 0.18μm high-voltage CMOS technology was demonstrated. In order to control the floating gate (FG) potential so as to put and pull electrons in/out of FG, two isolated n-wells are required to serve as the program/ erase gates, respectively. The design with two independently biased n-wells greatly increases the overall cell size. Besides, voltages that can be applied on these well-based coupling gates are limited by breakdown voltage of the n-well-to-substrate junctions [4]. FinFET technologies not only allow us to realize the proposed cell more compactly, where highly area efficient coupling structures were brought about [5-6]. In this work, a sidewall erased MTP cell is proposed and investigated. In addition to the slot contact coupling structure, a contact erase gate further provides operation flexibility. Optimization of the cells' operation conditions as the array size enlarges is investigated comprehensively.

Cell Structure and Operation Principles

The proposed MTP cells investigated in this study are fabricated by 16nm-FinFET CMOS logic process. The program gate (PG), see *Figure 1(a)*, is composed of long contact slots closely placed on the sides of a metal FG on top of STI. While, a n-well with the FG laid on top functions as the erase gate (EG). The new cell illustrated in the *Figure 1(b)* features a short slot contact beside the FG as its erase gate (EG). *Figure 2* compares the cell layouts between the two, arranged in a NOR array. Through a contact erase gate, the new cell is 30% smaller than the conventional one following 16nm-node process design rules.

To enable data storage and erase of the floating gate cell, electrons are injected into the FG by CHEI (Channel Hot Electron Injection) and removed by Fowler-Nordheim (FN) tunneling. The pathway of removing electrons from FG is either through gate dielectric layer or via sidewalls between metal gate and contacts, as illustrated in *Figure 3(b)*. The basic cell operations are readily demonstrated by the threshold voltage change observed in the measured IV curves in *Figure 4*.

Measurement Results and Discussion

As shown in *Figure 5*, measured drain current drops as electron injection by CHE programming occurs, indicating a proper drain bias range. Time-to-program and time-to-erase characteristics in *Figure 6* under V_{PG} at 8V for programming and V_{PG} at -12V for erasing, respectively, are compared. Time-to-erase characteristics in *Figure 7* further indicated that the erasing through sidewalls between MG and slot contacts can be promoted with high V_{EG}. Under the read condition of V_{PG}=2V and V_{BL}=1V, the bit cell current can readily reach 20μA, see *Figure 8*, where state "1" represents the programmed state and "0" for the erased state. The proposed cells arranged in a NOR type array is illustrated in *Figure 9*, while its operation conditions are listed in *Table 1*.

Enlarged read windows obtained by lowering erase state V_T at the cost of increased leakage currents are shown in *Figure 10*. *Figure 11(a)* indicates that as the array size enlarges, number of cells sharing the same BL, *m*, increases. With flexibly adjusted V_{EG}, a good read window can be well-maintained as array sizes increases, as shown in *Figure 11(b)*. *Figure 12(a)* reveals the effect of PG coupling ratios (α_{PG}) on the read current difference between the selected and unselected cells. For an array with the number of WL= *m*, erase state's V_T can be push lower as α_{PG} increases to keep a read current ratio above 10. Disturb characteristics in *Figure 13* show that after 1k-cycle stress, the unselected cells remain undisturbed under the inhibit conditions outlined in *Table 1*. In *Figure 14*, endurance test results on the proposed cells demonstrates that a sensing window of 2V remains stable after 10k P/E cycles.

Conclusion

A fully compatible to FinFET logic process MTP memory, with slot contact coupling structure and a contact erase gate is proposed. A compact cell, good read window as well as reliable performance are demonstrated for NOR arrays, with the possibility of being scaled up readily.

Acknowledgements

The authors would like to acknowledge the support from Taiwan Semiconductor Manufacturing Company (TSMC) and Ministry of Science and Technology (MOST), Taiwan.

References

[1] Y.K. Lee, et al. IEEE NVSMW, pp. 26-27, 2008
[2] Y. Wang, et al. IEEE IOT, pp. 98-103, 2015
[3] Y.H. Yeh, et al. SSDM, 2018
[4] H.P. Zappe, et al. IEEE T-ED, pp. 335-343, 1987
[5] K. Zhai, et al. IEEE ICCCAS, pp. 430-434, 2013
[6] F.H. Meng, et al, JJAP, vol. 55, no. 4S, pp. 1-5, 2016

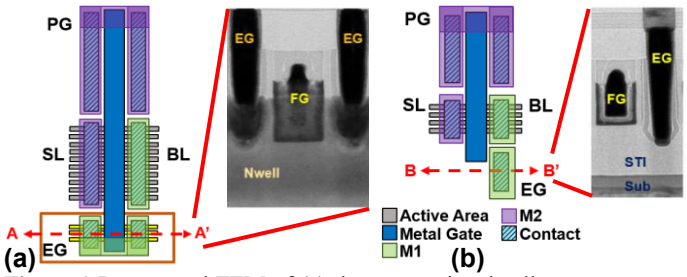


Figure 1 Layout and TEM of (a) the conventional cell and that of (b) the proposed cell investigated.

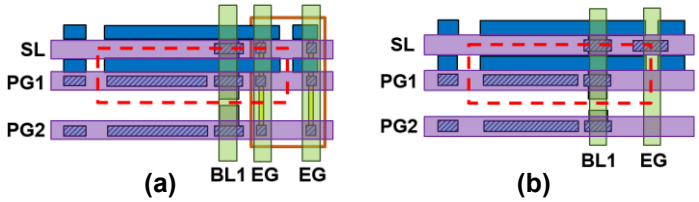


Figure 2 Layout examples of the conventional and the proposed cell arranged in a NOR array in 16nm node, showing 30% area saving.

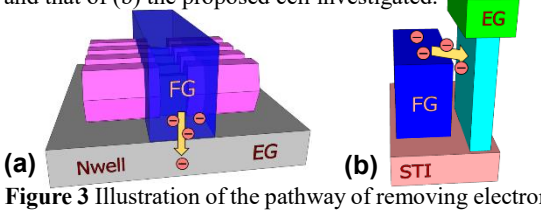


Figure 3 Illustration of the pathway of removing electrons from FG through (a) gate dielectric layer and that through (b) sidewalls between metal gate and contacts.

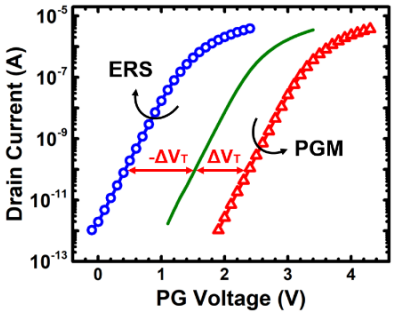


Figure 4 Basic program and erase of a cell are readily demonstrated by the threshold voltage shift observed after programming and erasing operations.

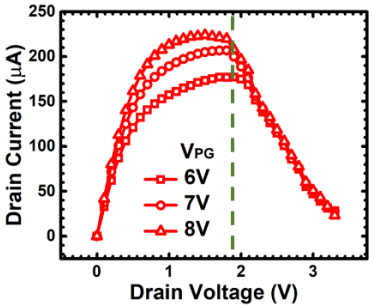


Figure 5 I_D drops as electron injection by CHE programming occurs, indicating an optimal drain bias range.

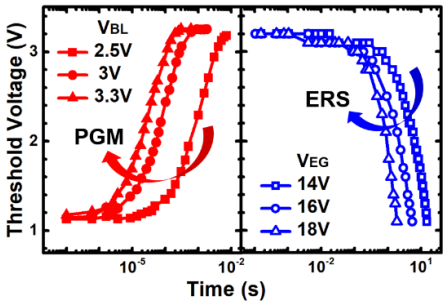


Figure 6 Time-to-program and time-to-erase characteristics for V_{PG} at 8V for programming and -12V for erasing, respectively.

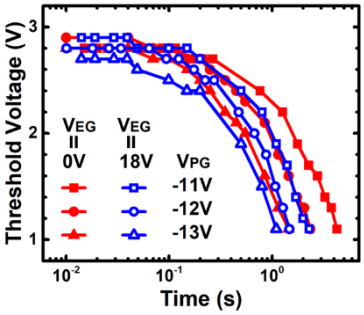


Figure 7 Comparison of the time-to-erase characteristics enabling erase through MG-Contact sidewalls.

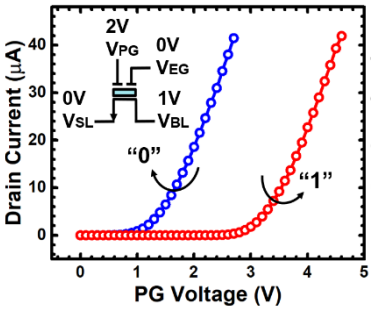


Figure 8 Under read condition of V_{PG}=2V and V_{BL}=1V, the sensing bit cell current can readily reach 20μA.

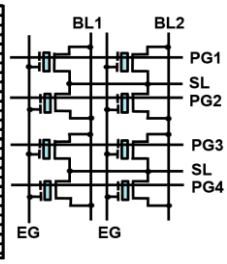
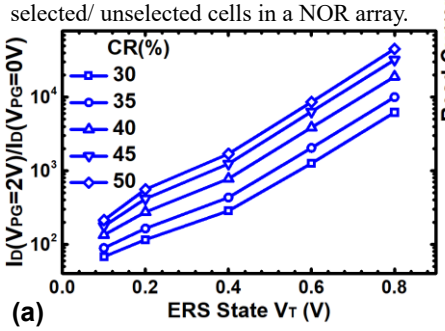


Figure 9 A sketch of the proposed cells arranged in a NOR type array.

	Read	Program		Erase
		Select	Unselect BL/PG	
PG	2V	8V	8V / 0V	-12V
EG	0V	0V	0V / 0V	18V
BL	1V	3.3V	0V / 3.3V	0V
SL	0V	0V	0V / 0V	0V

Table 1 Bias condition summary for selected/ unselected cells in a NOR array.



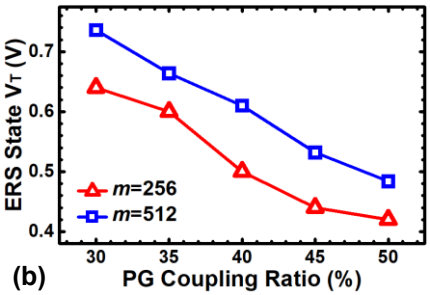


Figure 12 (a) Effect of PG coupling ratios (α_{PG}) on the current ratio btw the selected/unselected cells. (b)Erase states V_T can be push lower as α_{PG} increases, when read current ratio is kept at 10, m=216, 512.

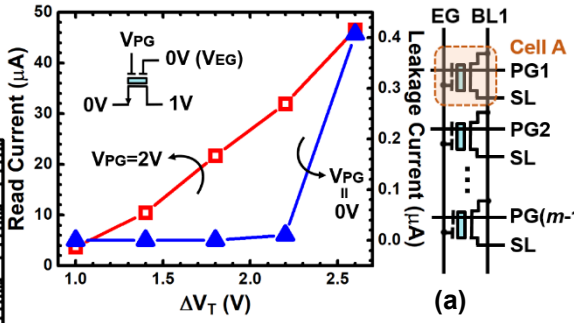


Figure 10 Larger read windows by lowering erase state V_T cost the increase of leakage currents on unselected cells.

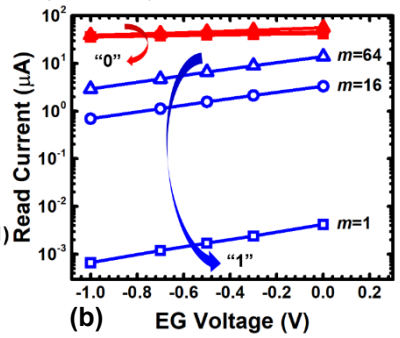


Figure 11 (a) As the array size enlarge, number of cells sharing the same BL, m, increases. (b) V_{EG} can be flexibly adjusted to maintain a good read window when m raises.

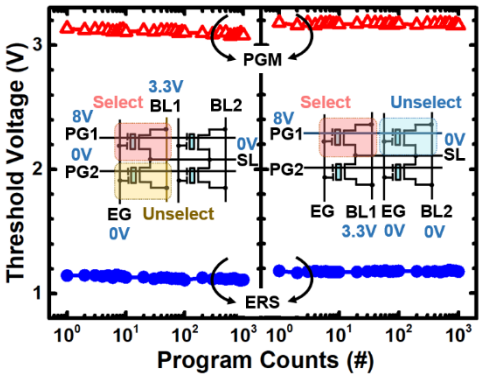


Figure 13 After 1k cycle stress, the unselected cells remain undisturbed under proposed inhibit operation conditions outlined in Table 1.

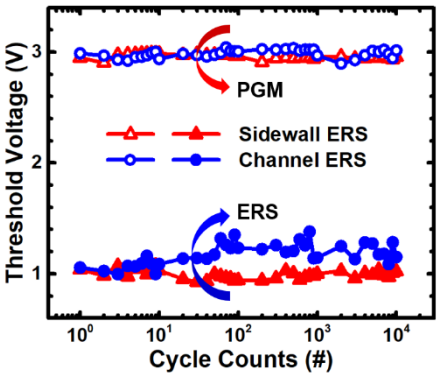


Figure 14 Endurance test of 10k P/E cycle counts on the proposed cells demonstrated that a sensing window of 2V can be kept.