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HfN Multi Charge Trapping Layers for Hf-based MONOS Nonvolatile Memory

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Abstract

The effect of HfN multi charge trapping layers (CTL) on the Hf-based Metal/Oxide/Nitride/Oxide/Si (MONOS) nonvolatile memory (NVM) characteristics was investigated to improve the threshold voltage (V_{TH}) controllability. The Hf-based MONOS NVM with $HfN_{1.3}/HfN_{1.1}/HfN_{1.3}/HfN_{1.1}$ 4-layer CTL realized precise control of flat-band voltage (V_{FB}) and V_{TH} compared to the Hf-based MONOS with $HfN_{1.1}$ single layer CTL. Furthermore, the retention characteristics were found to be remarkably improved for the Hf-based MONOS NVM with HfN multi CTL.

1. Introduction

High-k dielectrics is effective to realize high-speed and low-voltage operation for metal-oxide-nitride-oxide-silicon (MONOS) nonvolatile memory (NVM) [1]. We have reported the Hf-based MONOS NVM with high-k HfO_2 and $HfN_{1.1}$ dielectrics. The Hf-based MONOS structures were fully in situ formed to improve the interface property by the reactive sputtering utilizing Hf target. The MONOS structures are consisted from $HfN_{0.5}$ gate electrode, HfO_2 blocking layer (BL), $HfN_{1.1}$ charge trapping layer (CTL), HfO_2 tunneling layer (TL), and we have demonstrated the multi-bit/cell operation [2-4]. However, the V_{TH} controllability was necessary to be improved.

Tang et al. reported that the multi-layer CTL formed by the multi Zr silicate layers to improve the MONOS characteristics [5]. The multi-layer CTL was fabricated by changing the Zr and Si contents in each Zr silicate layer. The number of interfaces was increased in the CTL which led to increase the trap sites for the injected electrons.

In this paper, the effect of HfN multi-layer CTL for the Hf-based MONOS NVM was investigated to improve the threshold voltage (V_{TH}) controllability. The $HfN_{1.3}/HfN_{1.1}/HfN_{1.3}/HfN_{1.1}$ 4-layer CTL was fabricated by changing the N_2 gas flow ratio during the reactive sputtering. It is also expected that the equivalent oxide thickness (EOT) would be decreased because of the interface polarization effect [6]

2. Experimental Procedure

Figure 1 shows the experimental procedure used in this research. The Hf-based MONOS NVM was in situ formed on p-Si(100) substrate using the typical gate-last process [3]. After the active region formation and channel stop ion implantation, ion implantation was carried out for source and drain (S/D) regions (PH_3, $5x10^{15}$ cm^{-2}, 20 keV) [4]. Then,

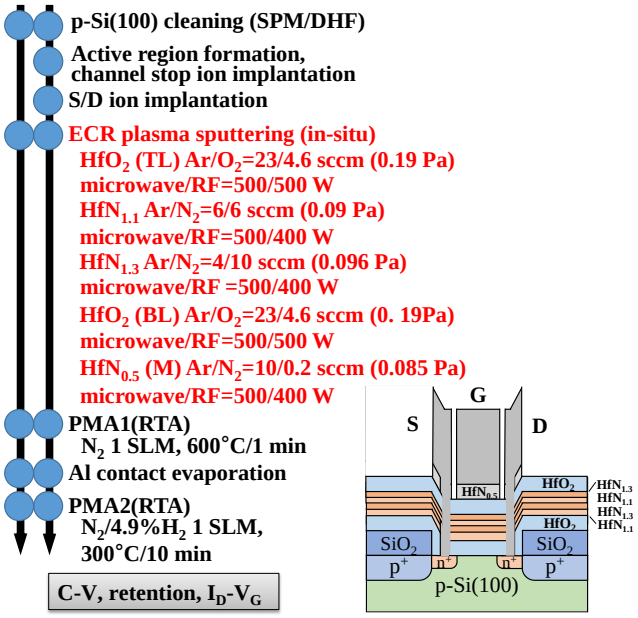

Fig. 1. Fabrication process and schematic cross-section of Hf-based MONOS NVM with multi CTL.

the $HfN_{0.5}/HfO_2/HfN_{1.1}/HfO_2$ (MONO) structure was in situ deposited on p-Si(100) by electron cyclotron resonance (ECR) plasma sputtering at room temperature (RT) [3]. The designed thickness of HfO_2 TL was 3 nm. The $HfN_{1.1}$ 1-layer CTL thickness was 2 nm. The $HfN_{1.3}/HfN_{1.1}/HfN_{1.3}/HfN_{1.1}$ 4-layer CTL was also fabricated with the thickness of 0.5 nm each. The thickness of HfO_2 BL and $HfN_{0.5}$ gate electrode was 8 nm each. Then, the post-metallization annealing (PMA1) was carried out at 600°C/1 min in N_2. After the contact hole formation and Al evaporation, PMA2 was carried out at 300°C/10 min in $N_2/4.9\%H_2$. The gate electrode size of the fabricated MONOS diodes was 100 x 100 μm^2. The gate length (L) and width (W) of the fabricated n-channel MONOS NVM was L/W = 10/90 μm.

The fabricated Hf-based MONOS diodes and NVMs were evaluated by C-V and I_D-V_G. The operation conditions were set as the program voltage/time (V_{PGM}/t_{PGM}) of 6 to10 V/1 s, the erase voltage/time (V_{ERS}/t_{ERS}) of -6 to -10 V/1 s at $V_D=V_S=0$ V. All the measurements were carried out at RT.

3. Results and Discussion

Figure 2 shows the program voltage dependence on the flat-band voltage (V_{FB}) shift in the C-V characteristics for the fabricated Hf-based MONOS diodes. The measurement frequency was 1 MHz. As shown in Fig. 2(a), the charge-

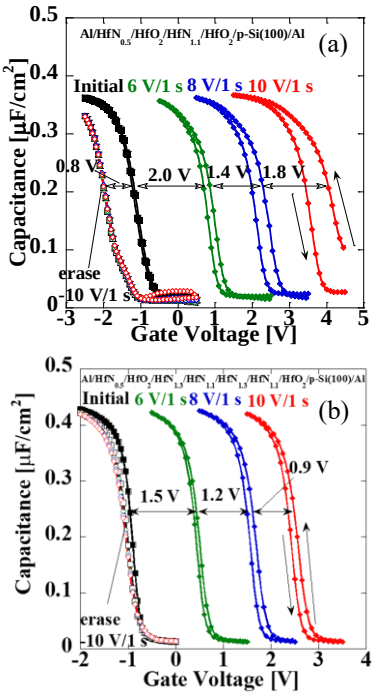

Fig. 2. V_{PGM} dependence on the V_{FB} shift for the fabricated Hf-based MONOS diodes with (a) 1-layer and (b) 4-layer CTL. The measurement frequency was 1 MHz.

injection type hysteresis width was increased with the program voltage, and V_{FB} shift was not stable with the program voltage in case of the Hf-based MONOS diode with 1-layer CTL. On the other hand, the hysteresis was markedly decreased even for the V_{PGM}/t_{PGM} of 10 V/1 s, and the V_{FB} was well controlled by the program voltage as well as the erase operation in case of 4-layer CTL. Furthermore, the EOT extracted by the dual frequency method was found to be decreased from 6.4 nm for the Hf-based MONOS with 1-lyaer CTL to 6.0 nm for the Hf-based MONOS with 4-layer CTL (not shown). This is probably caused by the interface polarization effect in the 4-layer CTL.

Figure 3 shows the comparison of retention characteristics for the Hf-based MONOS diodes. For the evaluation of retention characteristics, V_{PGM}/t_{PGM} of 10 V/60 s and V_{ERS}/t_{ERS} of -10 V/1 s were applied. Interestingly, the initial memory window (MW) was increased from 3.6 V with V_{PGM}/t_{PGM} of 10 V/1 s shown in Fig. 2(b) to 4.6 V for the Hf-based MONOS with 4-layer CTL probably due to the increase of trap states in the CTL. On the other hand, the initial MW was decreased from 5.2 V shown in Fig. 2(a) to 2.6 V for the Hf-based MONOS with 1-layer CTL. This is probably due to the de-trapping of the trapped electrons through the BL during the programing. The extrapolated MW to 10 years was decreased to 62% compared to the initial MW in case the Hf-based MONOS with 1-layer CTL, while it was 70% in case the Hf-based MONOS with 4-layer CTL.

Figure 4 shows the I_D-V_G characteristics of Hf-based MONOS NVM with 4-layer CTL. As shown in Fig. 4, the precise control of V_{TH} was realized with the program voltage

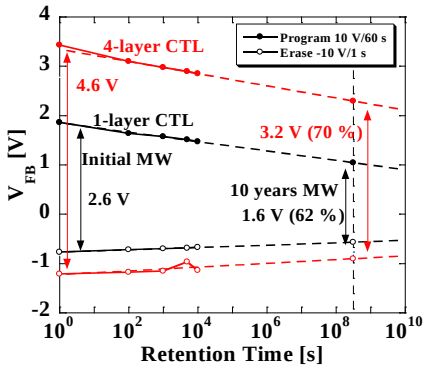

Fig. 3. Comparison of the retention characteristics for the Hf-based MONOS diodes.

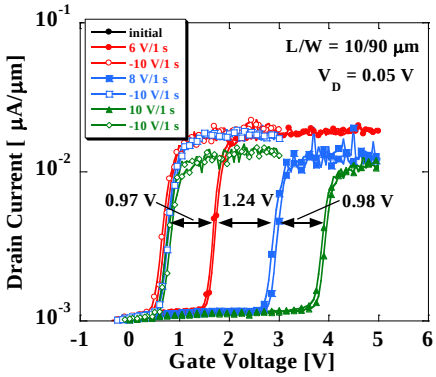

Fig. 4. I_D-V_G of n-channel Hf-based MONOS NVM with 4-layer CTL.

from 6 V to 10 V as well as the erase operation which corresponded to the C-V characteristics shown in Fig. 2(b). Negligible hysteresis was observed and the saturation mobility of 180 $cm^2/(Vs)$ was obtained.

4. Conclusions

Hf-based MONOS NVM with HfN 4-layer CTL was investigated. The excellent V_{TH} controllability was demonstrated for the fabricated Hf-based MONOS NVM. Therefore, the Hf-based MONOS NVM with multi CTL is a promising device for the future analog memory applications.

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