Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp109-110

80nm tall thermally stable cost effective FinFETs for advanced DRAM periphery devices for AI/ML and Automotive applications

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Abstract

We propose a cost effective memory periphery platform based on tall fin, suitable for advanced DRAM memory. For the first time, functional and reliable tall fin (up to 80 nm fin height) are experimentally demonstrated. Significant Power and Performance improvement is achieved thanks to optimized thermally stable modules, such as S/D epi, gate stack, gate etch, junction schemes. Area advantages (>50% area gain) are shown in S/A area, making it a suitable solution for periphery devices of DRAM oriented to AI/ML, automotive and blockchain generation applications.

1. Introduction

Automotive, AI/ML and blockchain generation are imposing increasing demanding specs for DRAM memories [1]. Wider memory bandwidth can be achieved by using conventional planar SiO_2 mosfet and different interfaces, at the expense of energy per bit (e.g.: GDDR5 vs LPDDR4) [2]. Advantages of HKMG vs SiO_2/SiON planar DRAM periphery devices compatible with DRAM memory fabrication have been demonstrated [3, 4, 5, 6, 7]. Insights on power performance benefit of Finfet for DRAM peri devices have been discussed [8]. In this work we provide the first experimental validation of thermally stable, reliable tall fins (65nm and 80nm fin height). Power performance benefit vs fin height and expected area advantages on Sense Amp area are presented.

2. Experimental demonstration and Results

In this work, we have fabricated and benchmarked Si fin of different width and heights, tailored for DRAM periphery applications. TEM Cross sections of fin fabricated with Fin Height (FH) of 40nm, 65nm and ~80nm are shown (Fig 1).

DRAM memory integration flows typically require high thermal budget (in the order of several hours at 650ºC and above) [5], imposing specific modules development. Emulation of such thermal treatment is applied for all the fabricated devices, to prove the thermal stability. The gate stack is fabricated by using High-K/Metal Gate (HKMG) process flow based on Deposition and Gate Replacement (D&GR) [5]. Final Gate stack is composed by 1.1 nm of SiO_2, 2 nm of HfO_2, 5 nm of TiN.

Extended effective device width is achieved by increasing the fin height, resulting in larger current per footprint. Fig 2 compares Ion/Ioff for FH=65nm and 40nm, demonstrating an increase of +50% of Ion current for a given footprint, which trends with the effective width increase.

Tall fins (FH=80nm) require specific optimization of the Gate etch module with respect to more conventional short fins. An optimized chemistry based on SF_6/CH_2F_2 has been developed to properly etch the bottom part of the gate selectively to the fins. Achieved gate profiles for fin on top of active and on top of field are shown in Fig 3. Straight profiles are obtained, without fin attack and minimized TiN undercut.

TCAD process and device simulations have been used to optimize the device doping profile in 80nm tall fins (Fig 4b). DIBL improvement is shown with respect to 40nm fins (Fig 4d). Thanks to a thermally stable Source/Drain epi module (Fig 4a), significant current increase (~×2 ID_{lin}) is achieved, without penalty in electrostatics (Fig 4d). The resulting improved Ion/Ioff per footprint are confirmed by experimental measurements (Fig 5). Further device optimization is required to fully reap the benefit of enlarged device width.

Memory design requires multi Vth capability for power performance optimization. The proposed integration scheme is compatible with a thermally stable dipole Vth shifter approach. La/Al_2O_3 dipole shifters are successfully introduced as Vth shifter for N/PMOS across multiple channel length (Fig 6).

The impact of fin height on reliability was assessed with Positive and Negative Bias Temperature Instability measurements, at 125ºC (Fig 7). Taller fin exhibit lower trapped charge density during the respective BTI conditions than 30nm height fin, suggesting that the quality of the dielectric deposited on the walls of the taller fins is not compromised. Cap layers improve BTI reliability also on tall fins. The dielectric breakdown of these devices was compared by (constant ramp-rate) ramped voltage stress measurements, and shows similar Q_{bd} as a function of fin height, again inferring negligible impact of the tall fin processing on the subsequently deposited dielectric. Both N- and P-FET with cap layer shows lower Q_{bd}, believed to be related to the presence of the thin (breakdown-originating) cap layer, which results in the earlier breakdown of these stacks.

Tall fins maximize the effective width for a given footprint, increasing the area saving. However, an excessive fin height generates a detrimental impact on performance of the logic transistors. A compact model calibrated on experimental data and TCAD is used to simulate a NAND2 Ring Oscillators chain. Fig 9 shows the additional frequency gain obtained vs additional active power consumed, for increasing fin height. Multiple configurations are explored (low (1E16 at/cm^3) and high (1E19 at/cm^3) channel doping, 10 nm and 20 nm fin width, BEOL loaded and unloaded). While all the considered curves are positive till FH=80nm, beyond this value the additional fin height will start to increase power without generating frequency benefit on certain configurations.

Sense Amplifier (S/A) is a critical component of a DRAM memory, which absorbs a significant area of the entire chip [9]. The S/A area in a DRAM is defined by multiple transistors (NSA and PSA, Equalizer (EQ), Column Selectors (CSL)) as well as additional area overhead (due to N-P separation, landing contact ...). On top of the logic transistor area saving yielded by wider effective width of tall fin, additional area benefit can be achieved in the S/A area with threshold voltage mismatch benefit [8]. It has been demonstrated that HKMG planar can yield a 30% improvement in Avt compared to corresponding SiON planar device [4], and that FinFET can provide additional 30% benefit for the same gate stack with respect to planar [6]. Fig 10a) shows the expected device width gain in S/A (including NSA, PSA, EQ, CSL) of Fin vs planar HKMG, as function of Fin Height, for Fin Pitch (FP) 40nm and 80nm. (b) The real S/A lateral area gain is calculated for two overhead (OH) conditions (25% and 50%) mimicking two different design approaches. 80nm Tall fin grant ~×2 area gain, and tighter pitch (40nm) maximizes the lateral S/A area reduction to >×3 (Fig 10b).

3. Conclusions

We proposed a reliable, thermally stable cost effective Finfet based platform. This can be leveraged to improve power, performance and area of advanced DRAM peri devices.

Acknowledgements

We would like to express sincere thanks to all the imec IIAP Core Partners Program. Special thanks to Yangyin Chen and Teruyuki Mine (WD), Yusuke Higashi and Masamichi Suzuki (Kioxia) for the fruitful discussions.

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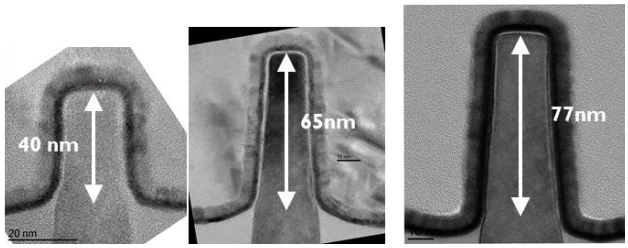

Fig 1: Example of fabricated HKMG Fin. TEM Cross section shown for 40nm, 65 nm and ~80nm tall fins

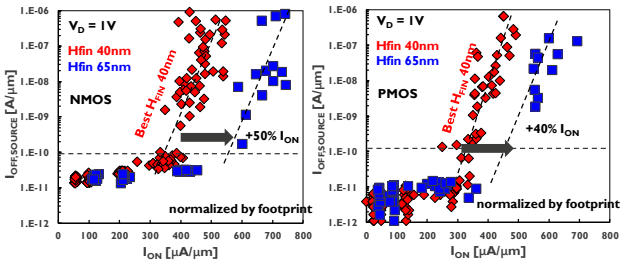

Fig 2: Ion/Ioff for 40 and 65 nm fin height, normalized per footprint. Increased current is achieved for both NMOS and PMOS

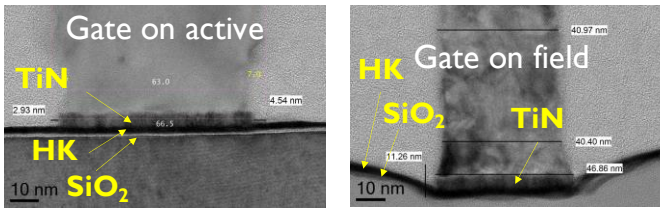

Fig 3: TEM Cross section for 80nm tall fins after patterning of Poly/TiN and HK etch, on top of active and on field. Achieved straight and controlled profiles after optimization are visible

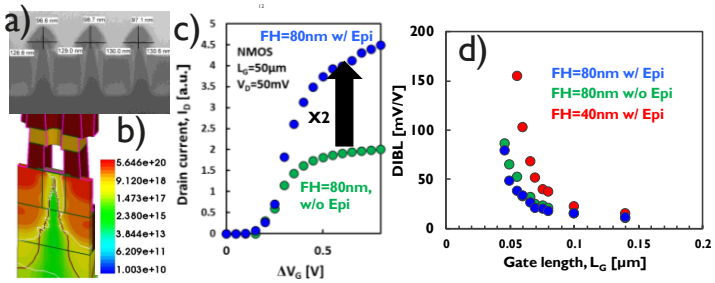

Fig 4: Optimized epi S/D and junction scheme for tall fin. a) Cross section of the thermally stable epi module b) TCAD Optimized Junction Doping Profile for FH=80nm. Exp data showing c) improved ID current and d) DIBL improvement wrt FH=40nm induced by optimized junction/epi

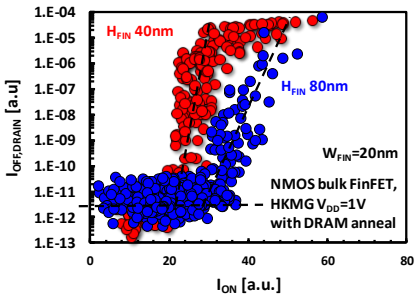

Fig 5: Ion/Ioff for 40 and 80 nm fin height, normalized per footprint (NMOS).

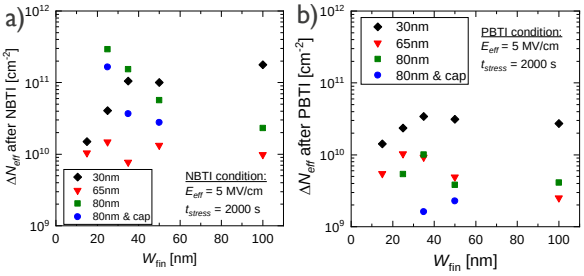

Fig 7: a) NBTI and b) PBTI measured at 125°C. Taller fins have lower trapped charge density. Capping layers further improve reliability

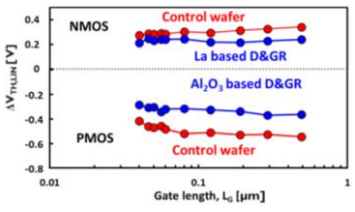

Fig 6: Vth shift achieved for NMOS/PMOS on tall fin thanks to La/Al_2O_3 capping layers

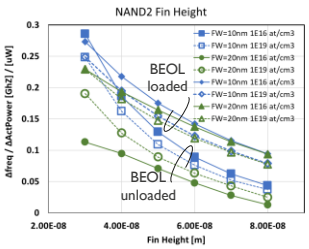

Fig 9: NAND2 RO freq. gain achieved vs additional Active Power consumed, as a function of FH.

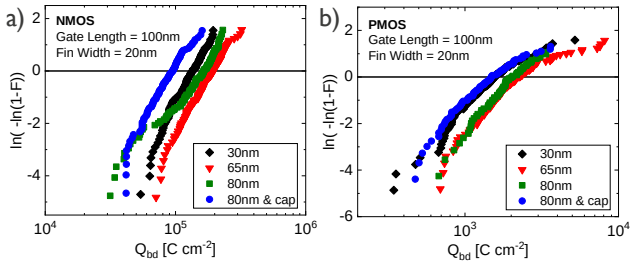

Fig 8: Dielectric breakdown extracted by ramped voltage stress measurements with constant ramp-rate. Similar Q_{bd} is extracted as a function of fin height

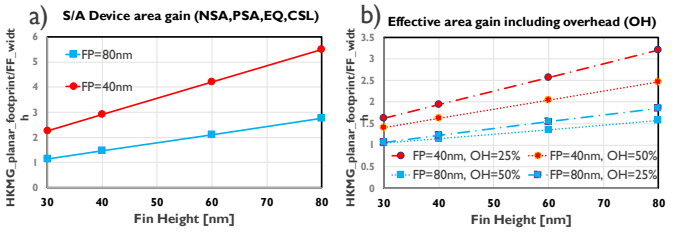

Fig 10: a) Total area gain (NSA,PSA, EQ, CSL sum) of Fin vs planar HKMG, as function of Fin Height, for Fin Pitch (FP) 40nm and 80nm, considering FF Avt [6]. (b) Total S/A lateral area gain, for two overhead (OH) conditions of 25% and 50%. Tall fin, tighter pitch maximizes the area gain