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Variability Analysis for Ferroelectric FET Nonvolatile Memories Considering Fluctuations due to Trapped Charges

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Abstract

This work investigates the impact of fluctuations due to interface trapped charges on memory window (MW) and read margin of the FeFET NVM under two scenarios: a uniform ferroelectric and random ferroelectric-dielectric (FE-DE) phase distribution. Our study indicates that the gate-width scaling of the FeFET will eventually be limited by the generated trapped charges. Under the presence of the FE-DE phase distribution, the impact of trapped charges is mainly on decreasing the mean MW (μMW) rather than increasing the MW variability (σMW) due to the interactions with the FE-DE phases. In addition, when down-scaling the interfacial layer thickness to increase μMW, the increased σMW due to the random interface trapped charges needs to be considered.

1. Introduction

With a CMOS-compatible HfO_2 based ferroelectric (FE) [1][2], ferroelectric field-effect transistor (FeFET) has garnered substantial interest as a candidate for next-generation NVM. Further scaling of the FeFET is crucial to the density of the NVM, and the random variability is expected to be important with the scaling of device dimensions. In this work, with the aid of TCAD atomistic simulation [3], we investigate the impact of fluctuations due to the interface trapped charges [2] on the aggressively scaled FeFET NVM. Our investigation of the trapped charge effect will also consider the random ferroelectric-dielectric (FE-DE) phase distribution of the ferroelectric layer [4].

2. Methodology

We consider acceptor-type interface traps at the mid-gap for an ultra-thin-body structure (Fig. 1(a)). For a given average trap density ($<n_T>$), the trap number in each device sample follows Poisson distribution and induces number fluctuation. The random pattern of a given trap number further results in position fluctuation as shown in Fig. 1(b). Regarding the FE-DE phase distribution, we use square grains with grain size = 6 nm to capture the effect [3]. Each grain has a certain probability to be DE (the DE probability = 20% in this work). After setting FE-DE phases and trap pattern independently, we apply square gate pulses with width = 100 ns and magnitude = -5 V and 5 V in writing operation for high-V_{th} state and low-V_{th} state, respectively. Both writing/reading operations are calculated based on the Preisach model for the FE [6].

3. Results and Discussion

Both number and position fluctuations of the trapped charges result in dispersive I_D-V_G curves with obvious V_{th} shift and subthreshold swing degradation as shown in Fig. 2(a), where the statistical mean and standard deviation (μ,σ) of the MW and read margin are extracted. In Fig. 2(b), comparing with the high-V_{th} distribution, the low-V_{th} distribution has larger V_{th} shift from the ideal case, which is qualitatively consistent with the data in [7] [8].

Fig. 3 shows the impact of trap variation on the MW and read margin with various thickness of IL (T_{IL}) for $<n_T> = 1\times10^{13}$ cm^{-2} and 3×10^{13} cm^{-2}, respectively. The high correlation (> 0.9) between the MW and read margin is independent of T_{IL}. It also reveals that the σMW to μMW ratio is nearly independent ($\sigma/\mu \approx 0.01$) of T_{IL} for $<n_T> = 1\times10^{13}$ cm^{-2}. Although thinner T_{IL} results in smaller voltage drop across IL and larger μMW, it also induces higher σMW, which is due to the higher local polarization difference between the no trap and with trap cases for thinner T_{IL}. Even for $<n_T> = 3\times10^{13}$ cm^{-2}, the ratio is still nearly constant ($\sigma/\mu \approx 0.03$) with various T_{IL}. This shows that the increased variability due to random traps needs to be considered in the down scaling of T_{IL}.

Fig. 4(a) compares the MW distributions induced by trap variation for devices with L_G/W = 12/24 nm and L_G/W = 24/12 nm. After examining the trap pattern for the worst 10% MW instances, we find that the region blocked by the traps along the W direction is the worst case pattern (Fig. 4(b)). This means that the impact of down-scaling W is larger than that of down-scaling L_G (μMW is smaller and σMW is larger for L_G/W = 24/12 nm as compared with the L_G/W = 12/24 nm counterpart). As $<n_T>$ increases from 1×10^{13} to 3×10^{13} cm^{-2}, the difference of (μMW, σMW) between W scaling and L_G scaling becomes even more. Besides, the high correlation between MW and read margin in Fig. 4(c) indicates that the trapped charge along the W direction is also the worst case pattern for read margin.

Fig. 5 considers fluctuations due to both the FE-DE phases and trapped charges (with $<n_T> = 1\times10^{13}$ cm^{-2}). The combined σMW (26.5 mV) is larger than the trap variation (12.3 mV), and is smaller than the FE-DE phase variation (33.3 mV). We have examined the interaction between the two variation sources and found that there are two kinds of interaction as illustrated in Fig. 6. First, the interface trapped charges may emerge under the FE grains and reduce the polarization. On the other hand, the trapped charges may also emerge under the DE grains and decrease the leakage, thereby enhancing the polarization. These interactions explain why the σMW induced by combined variations can become smaller than that induced by the FE-DE phase variation.

In Fig. 7, the combined σMW is smaller than the FE-DE phase variation with the down-scaling of channel area. For the dispersion of read margin, gate-width scaling (L_G/W = 24/12 nm) is still serious due to higher position fluctuation. For MW distribution, the trapped charge effect is the difference of the FE-DE phase variation and the combined variation, and it is mainly on μMW rather than σMW.

In Fig. 8, we can see that the combined σMW slightly decreases as $<n_T> = 1\times10^{13}$ cm^{-2} (as compared with the FE-DE phase variation), but increases as $<n_T> = 3\times10^{13}$ cm^{-2}. As $<n_T>$ continues to rise, most of channel carriers are screened away from the interface, which makes the aforementioned interactions weakened. Therefore, the σMW eventually increases with the increasing trap number fluctuation.

Acknowledgements

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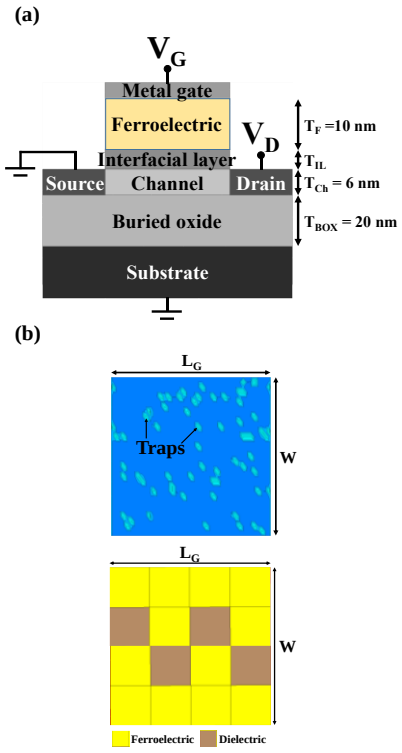

Fig. 1 (a) Schematic of the n-type FeFET in this study. The FE is placed on top of the interfacial layer (IL) of an UTB channel. (10 nm HZO, P_r = 20 μC/cm^2, P_S = 23 μC/cm^2, E_C = 1.5MV/cm [5]) (b) An instance of trap and FE-DE phase pattern in a device with L_G/W = 24/24 nm.

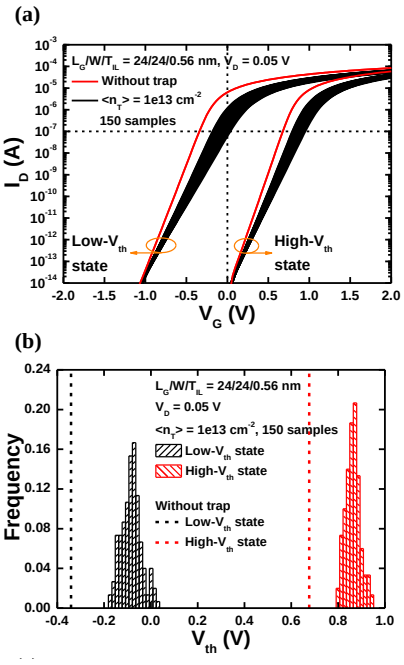

Fig. 2 (a) I-V dispersions for both high-V_{th} and low-V_{th} states. The MW can be extracted from the difference of the threshold voltages at $I_D = 10^{-7}$ A, and the read margin can be determined at V_G = 0 V. (b) V_{th} distributions of the two states due to the interface trapped charges.

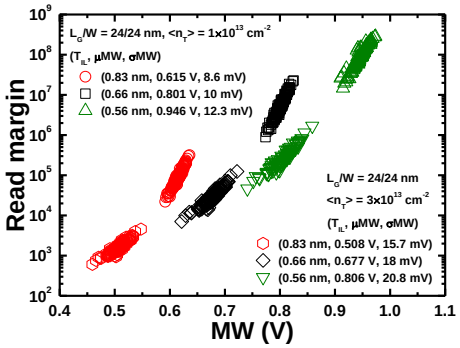

Fig. 3 Scatter plots of MW and read margin for FeFETs with various T_{IL} under $\langle n_T \rangle = 1\times10^{13}$ and 3×10^{13} cm^{-2}, respectively.

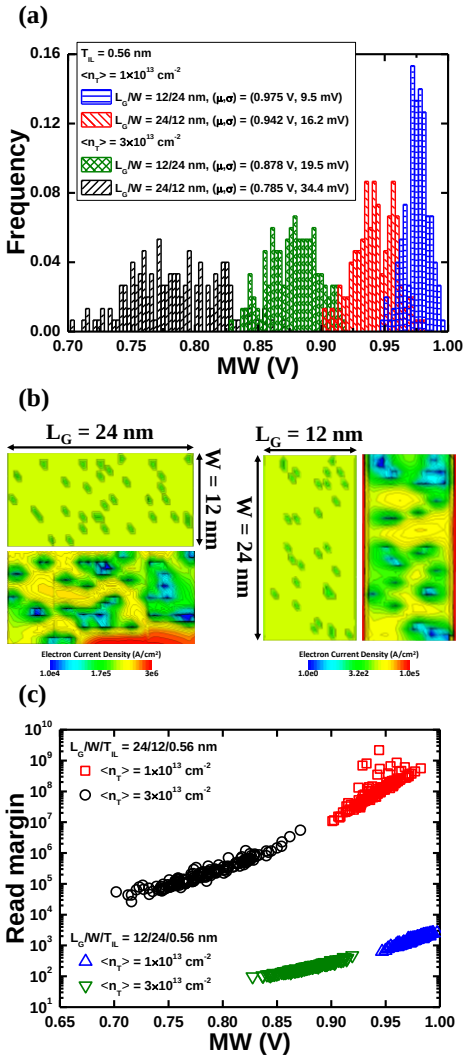

Fig. 4 (a) MW distributions due to the interface trapped charges with $\langle n_T \rangle = 1\times10^{13}$ cm^{-2} and 3×10^{13} cm^{-2} for scaled FeFETs with L_G/W = 24/12 nm and L_G/W = 12/24 nm. (b) Trap patterns and corresponding electron current densities at channel interface during read operation for the scaled FeFETs in (a) near the worst 10% MW tail under $\langle n_T \rangle = 1\times10^{13}$ cm^{-2}. (c) Scatter plot of MW and read margin for the scaled FeFETs in (a).

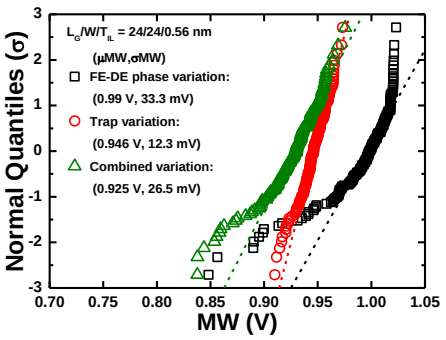

Fig. 5 Normal quantile plots of MW for the FE-DE phase, trapped-charge and the combined variations.

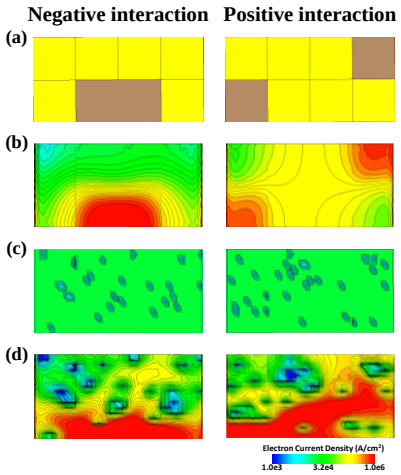

Fig. 6 Two kinds of interaction between FE-DE phases and trapped charges in the L_G/W = 24/12 nm device: (a) phase pattern (b) electron current density for phase variation (c) trap pattern (d) electron current density for combined variations.

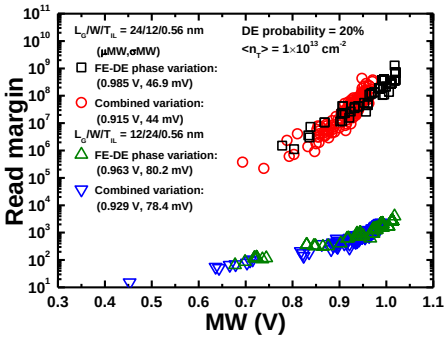

Fig. 7 Scatter plot of MW and read margin with various dimensions considering the combined FE-DE phase and trapped-charge variations.

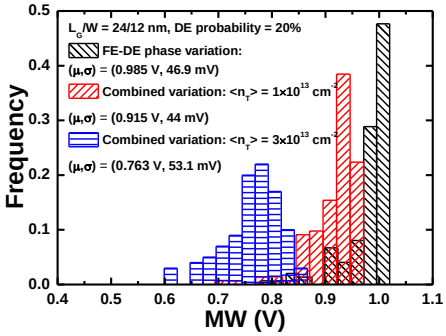

Fig. 8 MW distributions considering the combined FE-DE phase and trapped-charge variations.