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Design of a Magnetic-Tunnel-Junction-Based Nonvolatile Flip-Flop with Common-Mode Write Error Detection

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Abstract

Nonvolatile flip-flop (NVFF), which is one of the important components in the implementation of energy-efficient logic LSIs using nonvolatile devices, is required to be highly reliable in data store and restore operations. In this paper, we propose a highly reliable NVFF that can detect arbitrary errors that occur when storing data to the embedded nonvolatile memory. Through performance evaluation, it is shown that the proposed NVFF has a reliable error-detection capability with maintaining comparable performance of a conventional one in normal operations.

1. Introduction

With the advancement of IoT (Internet-of-Things) applications, a logic LSI design technology utilizing nonvolatile memory function of magnetic tunnel junction (MTJ) device has attracted attention [1]. By embedding a nonvolatile retention function in the LSIs, power gating to reduce leakage power can be performed with low overhead, resulting in highly energy-efficient LSIs.

Considering the stochastic behavior of MTJ devices [2] and demand for high-speed operation of nonvolatile logic LSI, the conventional basic logic gates such as nonvolatile flip-flops (NVFFs) [3] have an issue in the reliability of data store / restore operations. Some examples of highly reliable NVFF configurations that have a function to detect write errors in nonvolatile memory have been proposed [4], but they do not support all possible error conditions that may occur and are not sufficient to achieve this objective.

With these backgrounds, this paper firstly clarifies the vulnerability of NVFF to the stochastic behavior of MTJ devices, then introduces a new reliable NVFF configuration to solve this issue. Through the evaluation result, we demonstrate that the proposed NVFF designed using a 40-nm CMOS/MTJ-hybrid process technology can correctly detect all possible error conditions with less performance overhead.

2. Vulnerability of Conventional NVFF

NVFF normally operates as a flip-flop (FF), and when power gating is applied, two MTJ devices integrated in the NVFF hold 1-bit data as a nonvolatile memory (NVM) by taking a complementary resistance state. As shown in Figure 1, even if a sufficiently large write current with a long pulse width is adopted to MTJ devices, write errors sometimes occur due to the stochastic behavior of the device.

The error state of the MTJ devices after write operation is divided into two types: differential-mode state (write errors occur for both MTJ devices) and common-mode state (a write error occurs for only one MTJ device). The typical method of detecting write errors is to store the data written to the NVM to a latch for verification (balloon latch) and compare it to the value held in the FF [4]. However, as shown in Figure 2, the conventional method only considers differential-mode error. To ensure the reliability of NVFF, it is necessary to be able to detect both differential and common-mode errors.

3. NVFF with Common-Mode Error Detection Capability

Figure 3 shows the circuit schematic of the proposed NVFF, which operates in four different modes (flip-flop, store, restore, verify) based on the control signals. When the store operation is done correctly, (q, qb) and (q', qb') have the same value in the verify mode. As shown in Figure 4, when a pair of MTJ devices are in the common-mode error state, the potentials of P and Q drop to a certain value without a sufficient difference in the verify phase. Then, the circuitry indicated by red lines in Figure 3 is driven, and both q' and qb' become low. Thus, by comparing the voltage levels of terminals (q, qb) and (q', qb'), the common-mode error can be stably detected. Similarly, a differential-mode error can also be detected.

4. Evaluation Result

Figure 5 shows simulated waveforms of the proposed NVFF designed using a 40-nm CMOS/MTJ-hybrid process. We have confirmed that the proposed NVFF not only operates in the appropriate mode according to the control signal, but also correctly detects common-mode errors. In addition, as shown in Table 1, we have confirmed that the performance of the proposed NVFF under normal operation is comparable to conventional NVFFs that do not have common-mode error detection capability.

5. Conclusion

The proposed NVFF, which has the ability to detect arbitrary errors in store operations, is a key technology for achieving reliable operation of high-performance and energy-efficient nonvolatile logic LSIs. As a future prospect, we will implement a nonvolatile logic LSI with a number of proposed NVFFs and their control circuits, and evaluate their system-level performance.

Acknowledgements

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References

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[2] A. Fukushima, et al., APEX, 7, 083001 (2014).
[3] N. Sakimura, et al., ISSCC 184 (2014).
[4] K. Usami, et al., NVMSA, 91 (2018).

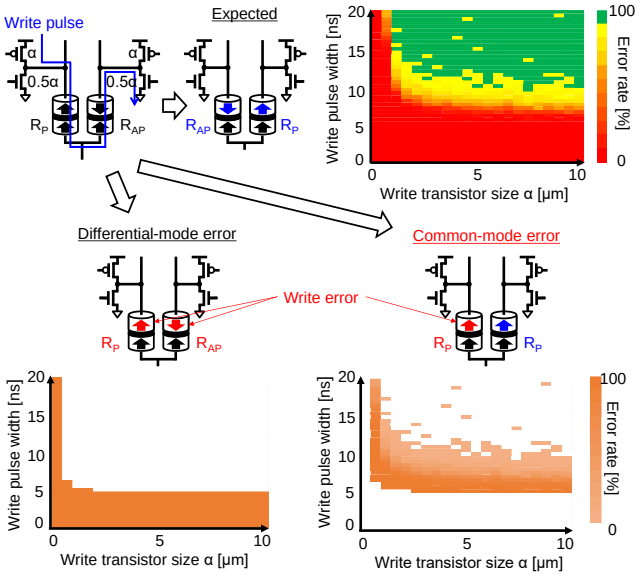


Fig. 1 Relationship between write pulse width, write transistor size and write error probability in NVFF, and breakdown of error modes.

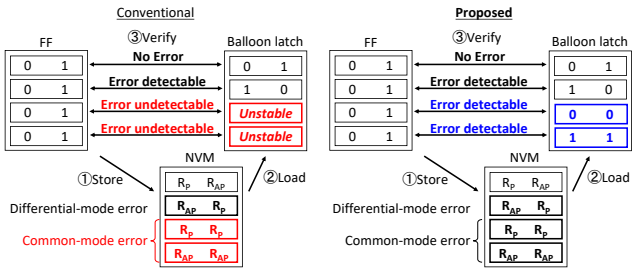
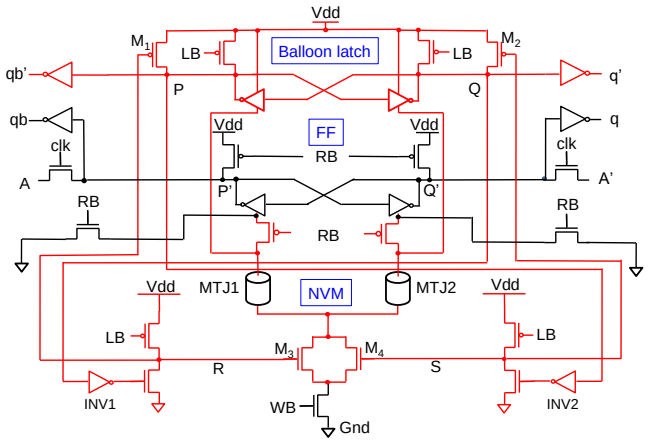


Fig. 2 Reliability of (a) conventional and (b) proposed NVFF in PG.



Input					NVM		Output				Function
A	A′	WB	LB	RB	MTJ1	MTJ2	q	qb	q′	qb′	
D	$\overline{D}$	1	1	1	-	-	D	$\overline{D}$	-	-	Flip-flop
		0	1	1	R_D	$R_{\overline{D}}$					Store (Success)
					$R_{\overline{D}}$	R_D					Store (diff. error)
					R_D	R_D					Store (comm. error)
		1	0	1	R_D	$R_{\overline{D}}$			D	$\overline{D}$	Verify (no error)
					$R_{\overline{D}}$	R_D			$\overline{D}$	D	Verify (diff. error)
					R_D	R_D			0	0	Verify (comm. error)
		1	0	0	R_D	$R_{\overline{D}}$			D	$\overline{D}$	Restore

$(R_D, R_{\overline{D}}) = (R_P, R_{AP})$ *when* $D = 0$, $(R_D, R_{\overline{D}}) = (R_{AP}, R_P)$ *when* $D = 1$

Fig. 3 Proposed nonvolatile flip-flop and its truth table.

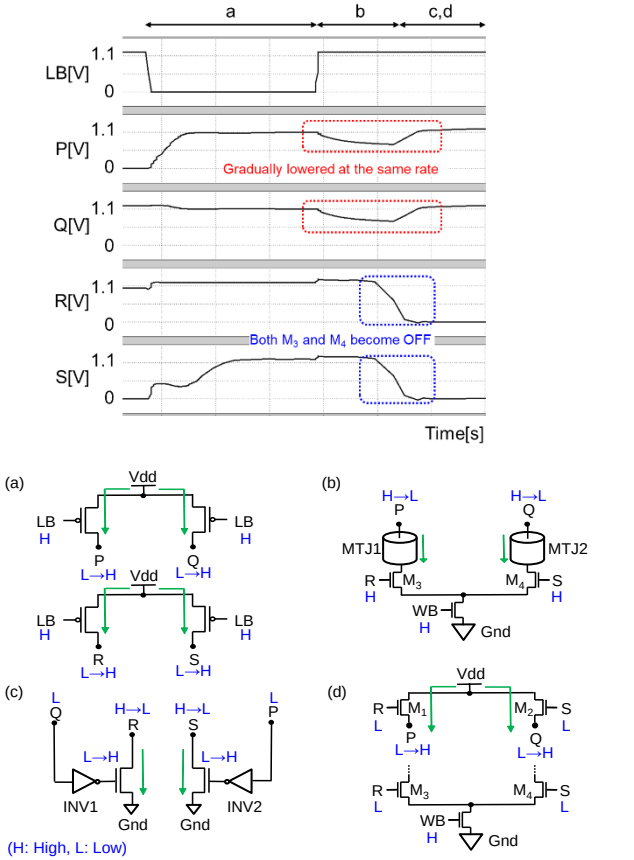


Fig. 4 The flow of detecting common-mode resistance state: (a) charge P, Q, R, and S, (b) discharge P and Q at the same rate due to common-mode state of two MTJs, (c) discharge R and S by sensing the potential drop of R and S below threshold, (d) recharge P and Q.

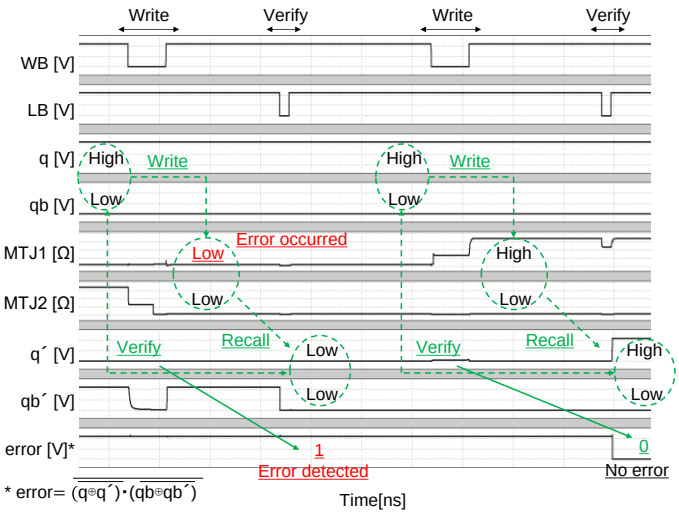


Fig. 5 Simulated waveform of the proposed NVFF.

Table I Performance comparison.

	Error detection function		Power [μW]			C-Q delay [ps]	Area [a.u.]
	Diff. error	Comm. error	Flip-flop	Verify (diff. error)	Verify (comm. error)		
[3]	No	No	0.232	N/A	N/A	66.4	1.00
[4]	Yes	No	0.353	64.1	N/A	69.6	1.33
This work	**Yes**	**Yes**	**0.359**	**67.1**	**74.5**	**69.8**	**1.89**