Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp101-102

STDP-like pulse response characteristics of interface dipole modulation FETs

Noriyuki Miyata

National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki, Japan
Phone: +81-29-861-2511 E-mail: nori.miyata@aist.go.jp

Abstract

The pulse response characteristics of multi-stack HfO_2/SiO_2 interface dipole modulation (IDM) FETs were investigated to explore the operation conditions of spike timing dependent plasticity (STDP). We demonstrate that the channel conductance potentiation and depression occur in response to the time difference between pre- and post-neuron spikes. We also examine the variation of IDM-based STDP response.

1. Introduction

The so-called deep learning with traditional artificial neural networks offers a variety of applications such as natural language processing and economic forecasting. This technique usually requires time-consuming learning tasks with large labeled datasets. On the other hand, unsupervised learning has also been studied for a long time. The spike timing dependent plasticity (STDP) observed in biological synapses is a promising synapse weight update mechanism for unsupervised spike neural networks (SNN) [1]. A simple example is a two-layer SNN system that recognizes the input image [Fig. 1], where synaptic weight changes according to feedback spikes from post-neurons. In the STDP learning, the weight changes depending on the time difference between pre- and post-spikes [Fig. 2]. Mimicking synaptic functions by scalable devices applicable to conventional silicon technology is one of the key challenges for building large STDP-based SNN systems [2]. In this study, we explore the STDP behavior using recently observed interface dipole modulation (IDM) from HfO_2/SiO_2 MOS stacks [3].

2. Concept of IDM-based STDP

Double-pulse control STDP operation of FET type memory, such as NOR flash memory and ferroelectric FET, has been widely studied, and most of them use bipolar triangular wave or a combination of triangular wave and rectangular wave as control signals [4, 5]. In this study, simple bipolar square waves were chosen to investigate the STDP behavior of IDM FETs.

The IDM FETs were fabricated by the gate last process. A multi-stack (MS) HfO_2/SiO_2 structure with six TiO_2 modulation layers was prepared on a HfO_2/Si substrate [Fig. 3]. The potential modulation induced at each HfO_2/SiO_2 interface is integrated, resulting in a threshold voltage (V_{th}) shift of the IDM FET. Hysteresis characteristics can be observed by DC I_d-V_g measurement [Fig. 4]. Here, the counterclockwise loop supports the IDM operation. The purpose of this study is to use this hysteresis behavior to find STDP-like conductance change.

3. Results and discussion

As expected from the I_d-V_g hysteresis above, the channel current either increase or decrease depending on the pulse polarity [Fig. 5]. Under this pulse condition, it is possible to modulate an order of magnitude. This change is dependent on the pulse voltage and period, as suggested in the previous paper [3]. That is, the IDM depends on the electric field strength and time applied to the interface. Under bipolar double-pulse conditions, similar changes occur when time differences (Δt) are given [Fig. 6]. When bipolar pulses are separately input to the two electrodes of the IDM FET, the maximum voltage applied to the gate stack changes according to the time difference. We can see that the conductance change of 50-pulse train depends on Δt. This result suggests that the conductance of IDM FET can be controlled by Δt.

The average conductance change during the 50-pulse train shows STDP-like potentiation and depression [Fig. 7]. However, this characteristic is slightly different from the biological STDP [Fig. 2]. The maximum and minimum conductance changes occur at the same positive and negative Δt as the pulse period, respectively. This difference can be improved by using triangle waves, but from the viewpoints of circuit simplification, we believe that the simple bipolar pulses used in this work are preferable. Here we calculated the conductance change using a simple MOSFET model and an electric-field-induced bond breakage/repair model previously proposed for TiO_2-modulator-based IDM [3]. By adjusting several parameters such as activation energy, a similar curve can be obtained, as shown by the dashed line in Fig. 7. Therefore, we believe that the observed STDP-like behavior is due to the IDM operation.

We should take note that rates of potentiation and depression in Fig. 6 are not constant during 50-pulse trains. The variations under the same double-pulse conditions were carefully examined [Fig. 8], which shows that the conductance modulation by the 50-pulse train also has a weak fluctuation. The distribution shown in Fig. 9 shows that peak positions of potentiation and depression can be separated, but each has a large distribution. In addition, this variation depends on the conductance itself. For SNN systems with IDM-based STDP, the impact of these variations on learning should be carefully taken account.

4. Conclusions

We demonstrated STDP-like behavior of IDM FET by using a double bipolar square pulse. We also suggested the importance of variation observed from the potentiation and depression characteristics.

Acknowledgements

This work was supported by JSPS KAKENHI Grant Number 16H02335 and 19H02178. Part of the device fabrication was conducted at the AIST Nano-Processing Facility (AIST-NPF).

References

[1] D. E. Feldman, *Neuron* **75**, 556, (2012).
[2] K. Roy, A. Jaiswal, P. Panda, *Nature* **575**, 607 (2019).
[3] N. Miyata, *Sci. Rep.* **8**, 8486 (2018).
[4] G. Malavena, M. Filippi, A.S. Spinelli, C.M. Compagnoni, *IEEE Trans Electron Devices* **66**, 4733 (2019).
[5] S. Oh, C.-H. Kim, S. Lee, J. S. Kim, J.-H. Lee, *Nanotechnology* **30**, 435206 (2019).

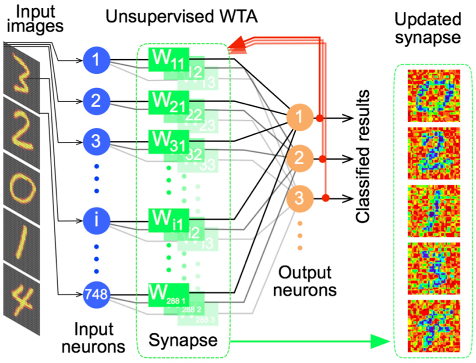

Fig. 1 Example image recognition system of two-layer SNN with unsupervised learning. Synaptic weights are updated by feed-back spikes from the output neurons.

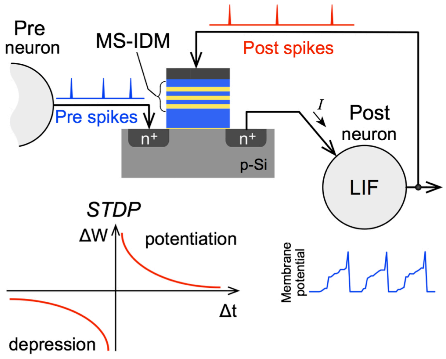

Fig. 2 STDP-based learning with multi-stack (MS) IDM FET. Channel conductance changes depending on time difference between pre- and post-spikes.

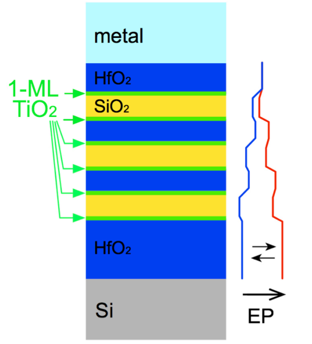

Fig. 3 Fabricated MS-HfO_2/SiO_2 IDM gate stack with six TiO_2 modulation layers. Potential change of each interface contributes to the threshold voltage shift of IDM FET.

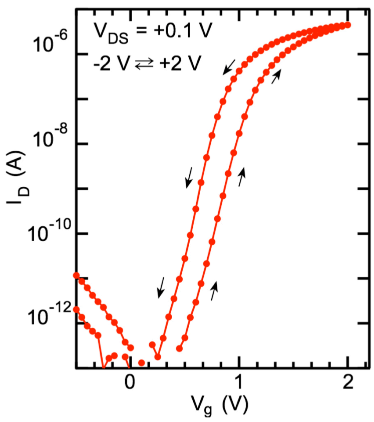

Fig. 4 I_d-V_g hysteresis curve observed from MS-HfO_2/SiO_2 IDM FET. Counterclockwise loop induced by IDM is used for STDP operation in this work.

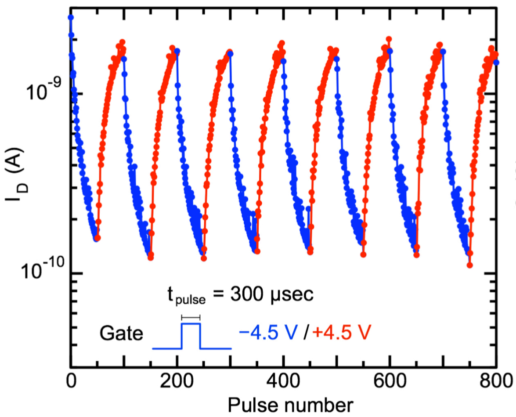

Fig. 5 Pulse response characteristics of MS-IDM FET. Pulse voltage polarity input to gate electrode is inverted every 50 pulses and channel current is read at $V_g = +0.6$ V

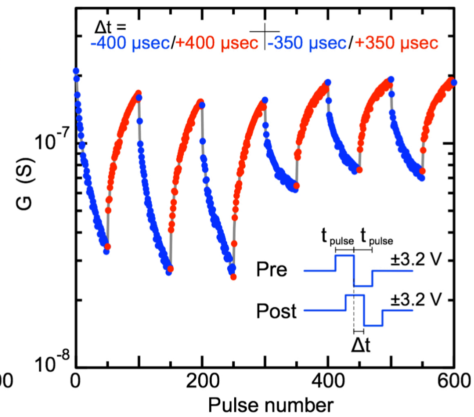

Fig. 6 Double-pulse-induced conductance changes of MS-IDM FET. Pre- and post-bipolar square-wave pulses with time difference (Δt) are separately inputted to IDM FET.

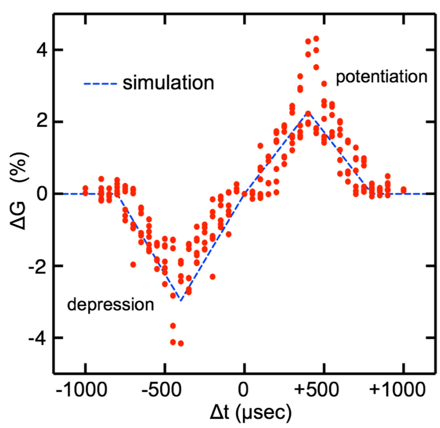

Fig. 7 STDP-like potentiation and depression of double-pulse-induced conductance change (ΔG). ΔG averaged over 50-pulse trains are plotted.

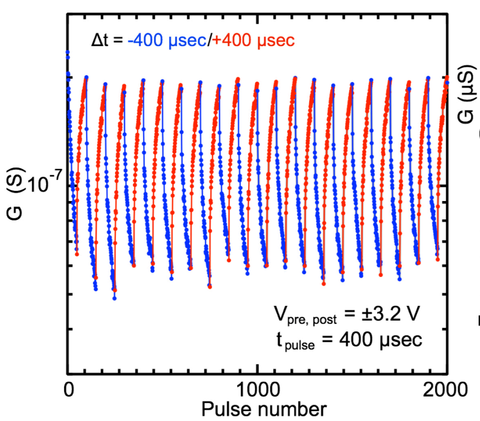

Fig. 8 Cyclic double-pulse STDP measurement for $\Delta t = \pm 400$ μsec. Weak fluctuation takes place in the conductance change even under the same pulse conditions.

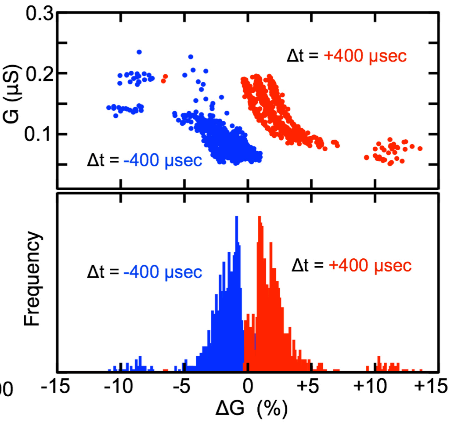

Fig. 9 Potentiation and depression conductance change (ΔG) distribution estimated from cyclic double-pulse measurement in Fig. 8. Upper plot shows that ΔG depends on G.