 Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp117-118

Novel low k Dielectric materials for nano device interconnect technology

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Abstract– Mechanically robust low k C-rich SiCN and pSiCN dielectrics with excellent built-in Cu oxidation and diffusion barrier have been developed and evaluated as potential alternative low k Interlevel dielectrics for Cu interconnects. The novel low k dense C-Rich SiCN (k=3.3) and lightly porous C-Rich SiCN (k=2.8) films have high modulus (E~> 15-30 GPa) and significantly lower Plasma Induced Damage (PID) as compared to typical pSiCOH (k~2.4-2.7) dielectrics. The excellent Cu diffusion barrier properties of these SiCN dielectrics enable the use of thinner metallic Cu barriers that resulting in larger Cu line's volume, reduced resistance and overall improved RC in sub-50 nm pitch interconnects without TDDB and EM reliability penalty.

I. Introduction

With device scaling, the need for reducing BEOL RC delay becomes increasingly important[1,2]. Lower dielectric constant k (lower C) of pSiCOH[3,4] material impacts TDDB performance. Mechanical strength, plasma induced damage (PID) integration challenges, pattern collapse and reliability requirements of pSiCOH materials for future nano fabrication has been a great concern[5,6,7]. This paper reports the development and optimization of novel PECVD dense C-rich SiCN (k=3.3) and lightly porous SiCN (k=2.8) low k dielectrics targeted for sub-50nm pitch Cu-Low k CMOS BEOL . These novel dielectrics were successfully implemented in multilevel sub-50 nm pitch Cu-low k BEOL with half of the standard metal liner/barrier thickness for significant reduction in RC while maintaining good TDDB and EM reliability.

II. Experimental

The C-rich SiCN films were deposited in a commercially available 300 mm PECVD system using Trimethyl Silane (TMS) + NH_3 and C_2H_4 at 350°C using 13.56 MHz RF frequencies. The lightly porous C-rich SiCN was deposited in the same system at 250°C using carbon-rich cyclic dimethyl-silacyclopentane (DMSCP) precursor and NH_3, and then subsequently cured with UV at 350°C. The deposited dielectric films were characterized by various analysis techniques and then compared with reference pSiCOH[4] (k=2.45). Multilevel sub-50 nm pitch CMOS BEOL Cu-low k device structures were fabricated with these low k C-Rich SiCN (k= 2.8, 3.3) and pSiCOH dielectrics with various liner thicknesses for reliability performance and overall RC reduction evaluation.

III. Characterization of C-Rich SiCN/p-SiCN Films

Table 1 summarizes various properties of a high performance pSiCOH[4] and novel C-Rich SiCN (k=3.3) and p-SiCN (k=2.8). The modulus of C-Rich SiCN and pSiCN are 2-4x (E=14-34 GPa) higher than those of pSiCOH (E=7-8 GPa). The C-Rich SiCN dielectrics have good Cu diffusion barrier properties as well as excellent oxidation barrier properties as compare to a pSiCOH film at 200°C, 24 hrs air exposure. SiCN and pSiCN dielectrics have no oxygen source for the metal and metal liner oxidation and need no adhesion layer to produce good adhesion (>= 4MJ/cm2) to other metals and dielectrics[8-9]. The PID[4] of SiCN dielectrics arelower than the best carbon rich pSiCOH 2.45, table 1. Thus, SiCOH dielectrics will have more sidewall damage by preclean, RIE and PVD processing and subsequently high keff value (>=20%).

IV. SiCN dielectrics: Modeling and Device Fabrication

In sub-50 nm pitch Cu-low k BEOL, thick PVD liners (>=5 nm) are normally needed to suppress EM induced mass flow, improve adhesion[10, 11] and achieve the needed reliability performance. This will result in a smaller Cu volume, exacerbates the known increase Cu resistance with smaller Cu lines and subsequently increase overall RC. Figures 1A-1C show the typical M_2 level Cu-SiCN (k=3.3) dielectric stacks and analysis as following: (A) STEM of fabricated structure of "5nm" BEOL M_2 low k C-rich SiCN-CuMn (0.5% Mn) interconnect with no metal liner. (B) SIMS analysis showing no Cu diffusion (no Cu detected) into C-Rich SiCN and the formation of $MnSiO_x$ at interfaces.(C) EDX analysis confirms no Cu diffusion and no significant plasma damage to the dielectric. No copper was detected in the voltage sweep run, SIMS and EDX analyses. The CuMn(0.5% Mn) provides a small amount of Mn, enabling the growth of a self-forming barrier comprised of $MnSiO_x$ dielectric[10] as an additional Cu barrier. Figure 2 shows sub-50 nm pitch post CMP structures of Cu-high modulus SiCN, pSiCN and reference pSiCOH (k=2.45) dielectrics. SiCN and pSiCN show no flopdown or defects even at high aspect ratios (>=2) and small width/spacing dielectric patterned lines. This enables smaller dielectric lines, larger Cu lines/volume increase and subsequently a significantly lower R, and device's RC values.

V. Impact in RC and Device Reliability.

Figure 3 shows RC Reduction with no and reduced thickness liner/barrier for 48 nm pitch Cu-Low k SiCN BEOL M_2 structures with : no metal barrier, 1 nm and standard 6 nm metal liner. Overall, fatter Cu lines can be fabricated with SiCN with thinner liner for the same pitch dimension as compared to pSiCOH dielectric. The normalized wire and via resistance are reduced significantly with reduced liner thickness. For the SiCN dielectric with low PID, overall RC is improved significantly (>=30%).

The TDDB (5 MV/cm, 125 °C) test result of the M_2 structure indicates robust breakdown performance (Figure 4) with metal liner thicknesses of zero and 1/3 of standard thickness as compared to pSiCOH k=2.55 TDDB as references. No TDDB degradation (leakage performance or yield) as compared to standard pSiCOH dielectric was observed for SiCN with 10% smaller dielectrics spacing. Good EM performance with RC reduction in Cu-SiCN structure can be achieved with thinner 3.5 nm liner and selective Co cap/Co liner wrap around Cu structure[4,11], Figure 5.

V. Conclusion

Novel low k C-Rich SiCN and p-Si-Rich SiCN dielectrics with high mechanical strength, excellent Cu diffusion and good oxidation barrier properties have been developed and evaluated as alternative dielectrics for sub-50 nm Pitch Cu-Low k interconnects to minimize the dielectric patterned collapse, reduce PID and to achieve an overall RC reduction with thinner metal liner/barrier.

Acknowledgement: This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities.

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	Advanced pSiCOH	Novel Low k C Rich SiCN	
	pSiCOH	C-Rich SiCN	pSiCN
Precursor	OMCTS + UVcure	TMS+NH3+C2H4	DMSCP+NH3+UV
k (@ 150 for bulk	2.45	3.3	2.8
E (GPa)	8	34	~15-17
%C (by XPS)	28	~50 (without H)	~ 46 (without H)
Porosity (%)	18	0	~12-13
Blanket PID	0.31-0.35	0.125	0.189
Adhesion to Cu (J/m2)	4 to 4.13	> 4	>4
Graded layer for adhesion	~ 5-6 nm	0 (Not Needed)	0 (Not needed)
Cu Oxidation	poor	Good	Moderate

Table 1. Summary properties and comparison table of novel C-Rich SiCN/p-SiCN vs pSiCOH 2.45 film.

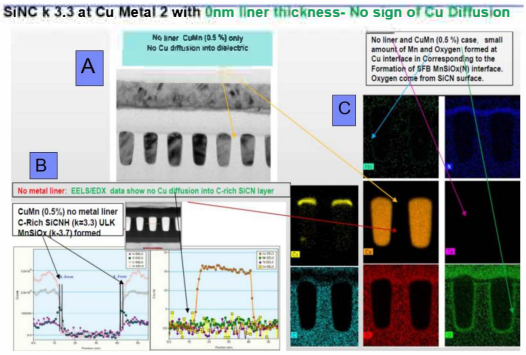

Figure 1. (A) STEM of BEOL M2 Low k C-Rich SiCN-CuMn with no metal liner. (B) SIMS study show no Cu Cu diffusion into C-Rich SiCN and MnSiOx at interfaces. (C) EDX confirms no Cu diffusion or signifiant PID.

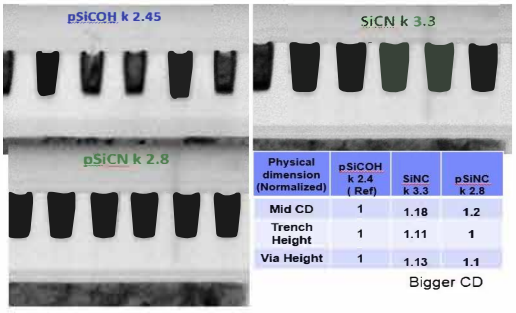

Figure 2. Typical sub-50 nm pitch STEM view and CD of post CMP of Cu-SiCN. pSiCN and pSiCOH 2.4 .

Liner	Normalized Line Resistance	Reduction Line Resistance (%)	Normalized Via Resistance	Reduction in Via resistance(%)
6nm liner (Ref)	1	0	1	0
1nm liner	0.84	16	0.52	48
No liner	0.68	32	0.14	86

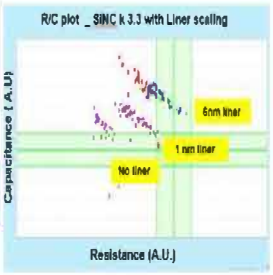

Figure 3. RC Reduction with no and reduced thickness metal liner : measured results for sub-50nm pitch Cu-Low k SiCN BEOL M2 structure.

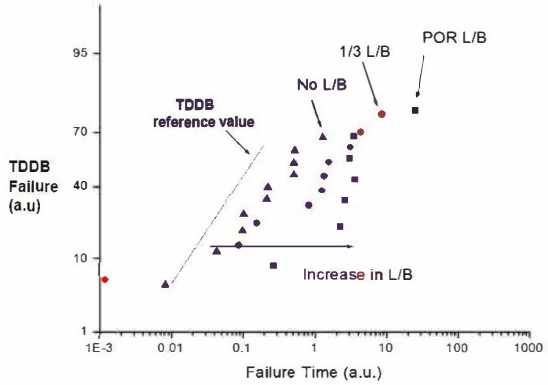

Figure 4- Robust Cu Diffusion and Oxidation barrier properties of SiCN improves sub-50 nm pitch TDDB of CuMn-SiCN even at thinner liner/barrier (L/B).

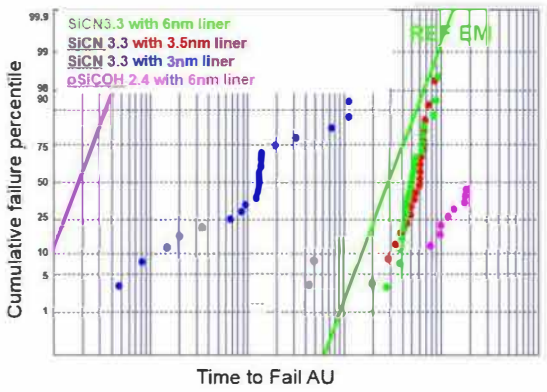

Figure 5. Electromigration performance of sub-50 pitch Cu-Low k SiCN with reference 6nm and thinner liner. Best EM is obtained with thinner 0.6x standard liner/ barrier with lower resistance and better TDDB than the reference pSiCOH k=2.45 with 6 nm liner.