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Development of Functional Interposer Using Bumpless Chip-on-Wafer - Feasibility Study of Voidless Bonding with Thin Adhesive -

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Abstract

To reduce the sizes of an interposer which is implemented with a capacitor chip and a re-distribution line (RDL), we are developing direct bonding without bumps using a chip-on-wafer (COW) process. No voids, even with a thin adhesive layer having a thickness of 5 µm, were achieved for the first time. We found that the occurrence of voids depends on the planarity due to the I/O pad structure of the capacitor and the viscosity of the adhesive material. This bumpless COW process enables us to reduce the total height to less than one-half compared with a conventional capacitor structure.

1. Introduction and Motivation

For highly integrated system level packages like multi-chip modules (MCMs), a miniaturized interposer including a capacitor is required, without sacrificing the functionality of power distribution networks (PDNs). In the case of conventional 2.5D systems for DRAM and MPU/GPU, passive devices are designed and bonded on the package substrates (PKG-SUB) using solder bumps, not on the Si interposer. The aim of this study was to reduce: (a) the surface area occupied by capacitors on the PKG-SUB, (b) the total thickness of the Si interposer and capacitors, and (c) RDL and interconnects between the capacitors and semiconductor devices, as shown in Fig. 1. In this paper, we describe the bonding of a thin capacitor to a thin adhesive layer developed for COW and wafer-on-wafer (WOW) processes with bumpless dual-damascene interconnects were used [1-2].

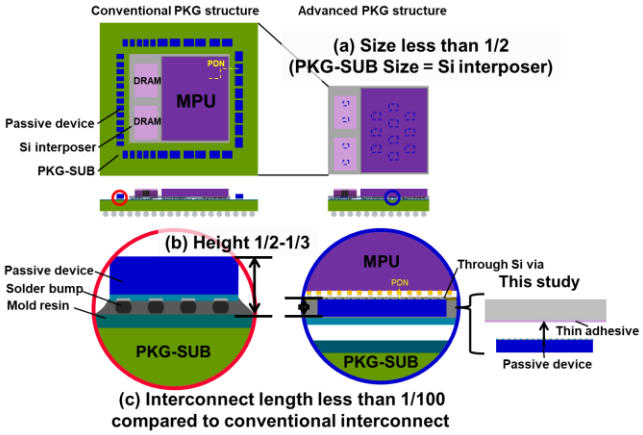

Fig. 1 Conventional and advanced package structure.

2. Experimental Procedure

Figure 2 shows the process flow of a functional interposer and chip bonding. A permanent adhesive material was formed by a spin-on technique to a thickness of 5 µm on a 300 mm glass wafer in order to allow defects to be observed from the back side after chip bonding. A Si chip and a Si capacitor chip having multiple terminal pads were prepared, as shown in Fig. 3. In the case of the Si capacitor, planarization using additional metallization and chemical mechanical polishing (CMP) was carried out. After bonding, the glass wafer was

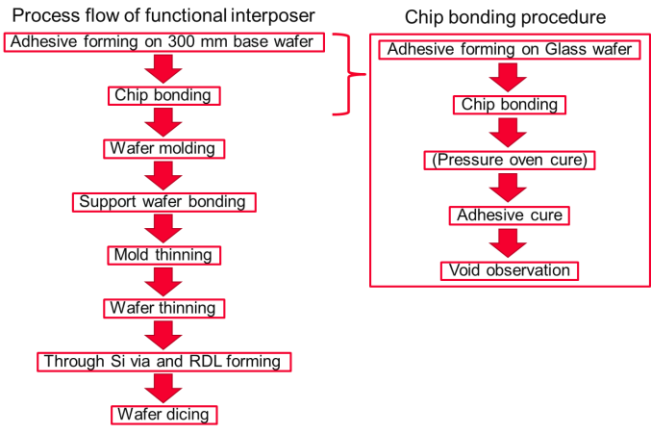

Fig. 2 Chip bonding procedure in process flow of functional interposer.

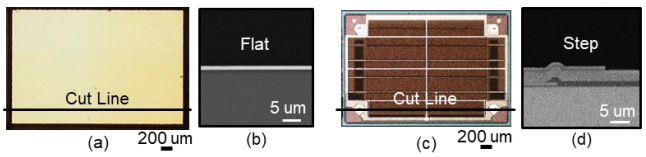

Fig. 3 Top and cross sectional views. (a) Si chip top view. (b) Si chip cross sectional view. (c) Si capacitor chip top view. (d) Si capacitor chip cross sectional view around I/O pad area.

processed by atmospheric pressure and heating, pressurizing and heating. Different pressurizing conditions, namely, a constant pressure and a cyclical pressure, were compared, as shown in Fig. 4. Voids and defects larger than 0.5 µm were observed in the adhesive layer by optical micrograph.

3. Results and Discussion

In case of the Si chip, voids were observed under atmospheric pressure and constant pressure (Condition A). No voids were observed by using the cyclical pressure (Condition B) as shown in Fig. 5. For the unprocessed Si capacitor chip, which had a 1.5 µm step height at the pads, a significantly large void was observed under Condition B as shown in Fig. 6 (a), whereas when using Condition B and planarization of the pad regions, no voids were observed as shown in Fig. 6 (b). Misalignment of the capacitor after bonding was within the accuracy specifications of the mounting machine. Figure 7 shows a cross sectional image of the Si capacitor chip after bonding. A thin adhesive layer without defects and exhibiting good bonding was observed. It is thought that voids were shrunk during the curing process and dissolved in the adhesive resin [3-4]. In this study, we thought that void reduction occurred due to lateral movement in addition to dissolving of voids in the adhesive resin. Since voids disappeared under the cyclical pressure condition, lateral movement of the voids predominantly occurred. Suitable conditions for the pressure and planarity of the bonding surface were found. The adhesive thickness was small, at 5 µm, with no bumps, and the total height after capacitor bonding became one-half as thin as that in a conventional capacitor chip with solder bumps. More details regarding void formation and the cause of their disappearance will be discussed.

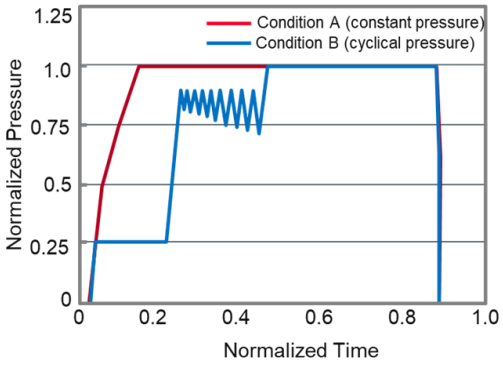

Fig. 4 Pressure profile in adhesive curing process.

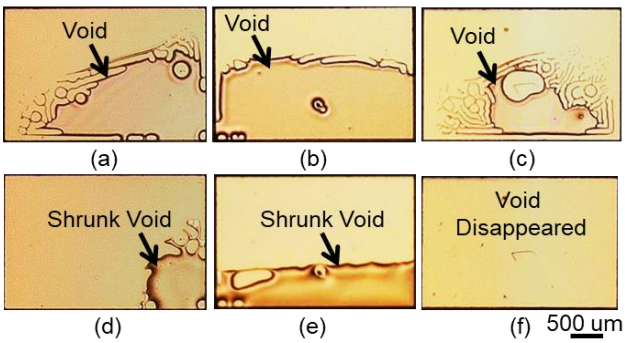

Fig. 5 Voids and defects larger than 0.5 µm observed images of Si chip surface. Convection oven cure condition as-mounted: (a), after cure: (d). Pressure condition A, as-mounted: (b), after cure: (e). Pressure condition B as-mounted: (c), after cure: (f).

Acknowledgements

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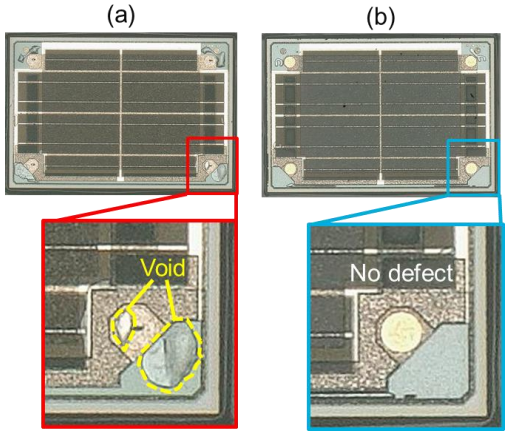

Fig. 6 Voids and defects larger than 0.5 µm observed images under pressure condition B:
(a) Unprocessed Si capacitor chip, (b) Si capacitor chip after planarization.

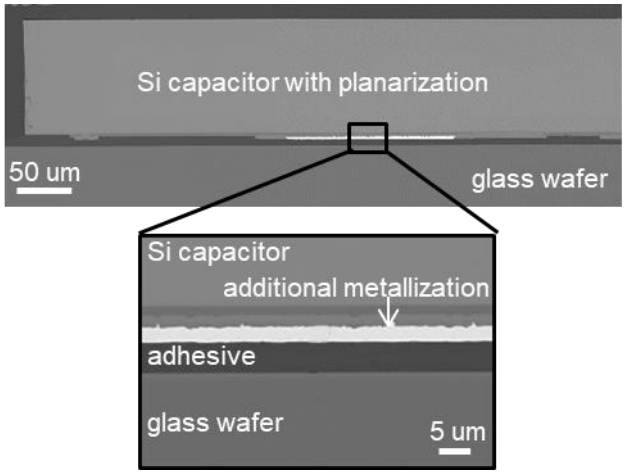

Fig. 7 Cross sectional image around bond pad of Si capacitor chip after planarization.