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Fabrication challenges in integrating self-assembled block copolymer process in semiconductor devices

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Abstract

We report the manufacturability challenges associated with integrating self-assembled block copolymer process (BCP) into process flows tailored towards thermal management in semiconductor devices. The role of surface roughness and process integration approaches on BCP pattern process is studied in detail in this work. Understanding the interdependence of process parameters on BCP pattern transfer can pave the way towards low cost, high volume manufacturing.

1. Introduction

Nanoporous membranes fabricated using electron beam lithography and directed self assembly (DSA) of block copolymer (BCP) process are reported to exhibit a reduction in thermal conductivity [1]. A ~6x reduction in thermal conductivity is reported for amorphous silicon nitride perforated with BCP [1]. Similar use of nanoporous membranes for heat dissipation and for improving thermal responsivity of MEMS beams have also been reported [2, 3]. However, for enabling directed self assembly for the lithographic pitch described in [1], advanced lithography processes are required. However, it is also reported in [1] that self-assembled BCP (without use of guide pattern) also exhibits a significantly low thermal conductivity (~5x reduction) compared to the reference device [1]. This opens up opportunities for exploring low cost nanopore fabrication process using self assembled BCP targeting MEMS and other thermal management devices. In this work, we explore the feasibility of integrating self assembled BCP process on a 200mm wafer to pattern silicon germanium and silicon nitride. The role of surface roughness, choice of hardmask and process sequence on final BCP pattern transfer is reported. In this work, a pitch of 40nm was targeted, however the learning can be fanned out to different pitches and different substrates.

2. Fabrication process flow

Test materials were fabricated in a 200mm pilot line at IMEC. 2um thick silicon oxide was deposited on a 200mm wafer. The oxide film was polished using CMP to reduce the surface roughness. This was followed by deposition of the layers to be patterned: (i) Stack of SiN was deposited where the silicon nitride film was deposited using a PECVD process at 400ºC (ii) SiGe film (65%Ge) was deposited using a thermal CVD process at 500ºC (wafer temp ~450ºC). An ALD based Al_2O_3 film was used as the hardmask to block the areas for the BCP pattern transfer. DUV lithography process was used to define the area to be perforated with BCP. Al_2O_3 film in these regions were etched using a dry etch process. Spin on carbon (SOC) and spin on glass (SOG) layers were subsequently coated onto these wafers to self-planarize the surface. This was followed by the spin coating of the BCP layer (PS-b-PMMA) and it involved two steps. (a) coating of an underlayer and (b) coating of the PS-b-PMMA matrix. The samples were subsequently annealed at 240ºC in an air ambient for 3 min. The etch process involved three steps: (i) selective etch of PMMA (ii) Etching of SOG/SOC hardmask and (iii) Etching of SiN or SiGe. After etching, remaining SOG/SOC is removed using a dry strip process. Al_2O_3 hardmask was later removed using a wet etch process. Schematic process flow used for BCP pattern transfer in both SiN and SiGe is described in Fig.1.

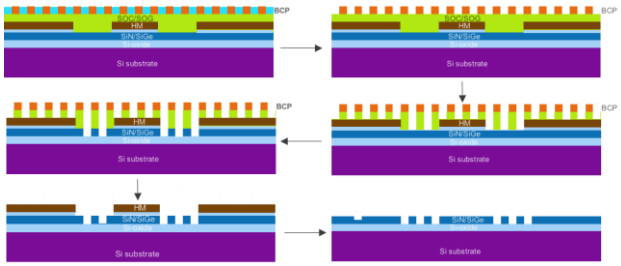

Fig. 1. Schematic of process flow used for integrating BCP for pattern transfer into SiN and SiGe

3. Experimental results and discussion

(a) Role of surface roughness on BCP pattern transfer

Angstrom scale roughness is reported to have an impact on self-assembly of block copolymers [4]. Understanding impact of surface roughness on the final pattern transfer process is critical in defining the choice of materials and the process scheme required to facilitate wafer scale manufacturing. Fig. 2 compares the surface roughness of two different silicon nitride films. The films differed in their deposition rates and the film deposited at a higher deposition rate showed a higher roughness range (Fig 2(a)) compared to one deposited at a lower rate (Fig.2(c)). The rms roughness was 2.5nm vs 1.5nm

respectively for these films. The higher roughness range translated into defect formation as shown in Fig.2(b). On migrating to low deposition rate SiN, defectivity was significantly reduced and the pattern was successfully transferred into SiN, as shown in Fig 2(d).

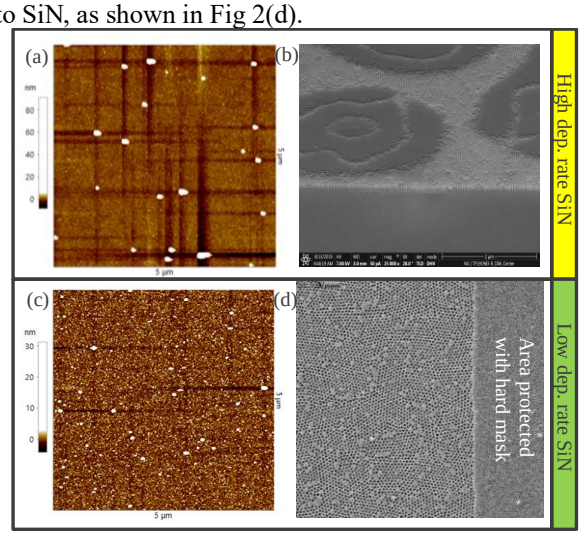

Fig.2. AFM data comparing SiN films with (a) high and (c) low deposition rate (b) SEM image showing defects after BCP patterning (d) SEM image after dry etch and hardmask removal for the low deposition rate SiN film.

In case of poly SiGe film, rms roughness was ~6.4nm whereas the roughness range was ~40nm. Despite the higher rms roughness, the overall defect density was lower compared to what was observed in SiN films (see Fig 3(b)). To improve the process further, a CMP step was added to smoothen the SiGe film prior to the BCP patterning process. The rms roughness was reduced to ~0.2nm, and as a result BCP patterns as shown in Fig 3(d) were obtained.

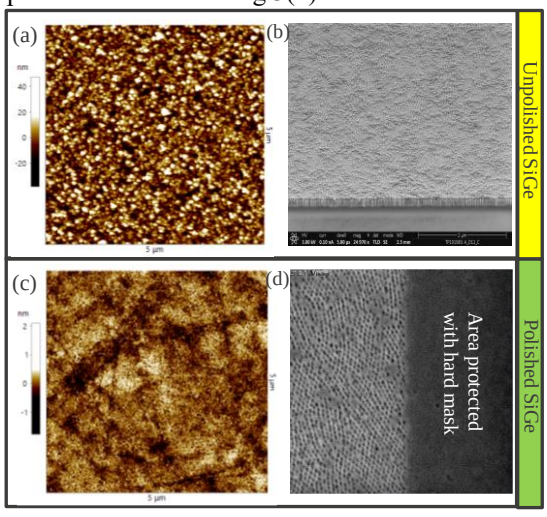

Fig. 3. (a, b) AFM of unpolished SiGe film (b) SEM of SiGe film after BCP etch (c) AFM of polished SiGe (d) SEM of SiGe film after BCP etch.

(b) Impact of process sequence on BCP pattern transfer

With any plasma process, there is always a risk of a surface damage, and we wanted to assess the impact of such plasma induced damage on the BCP pattern transfer process in SiGe. Fig.4(a) shows the results of pattern transfer when a dry etch was used for the Al_2O_3 hardmask opening. The damage at the corner is most likely due to micro trenching, as Al_2O_3 dry etch process can attack SiGe. On moving to a wet etch process for Al_2O_3 opening, there was no damage observed at the corners. However, BCP pattern imprints were observed in areas protected by hardmask, as seen in Fig. 4(b). This is attributed to the low selectivity between etch chemistries used to etch SiGe and Al_2O_3. To address these issues, a thin oxide layer was added in between SiGe and Al_2O_3. This oxide layer serves as a landing layer during the dry etch of Al_2O_3. The oxide layer is subsequently removed using BHF to ensure that there is no plasma induced damage on SiGe. The result of such a pattern transfer is shown in Fig 3(d).

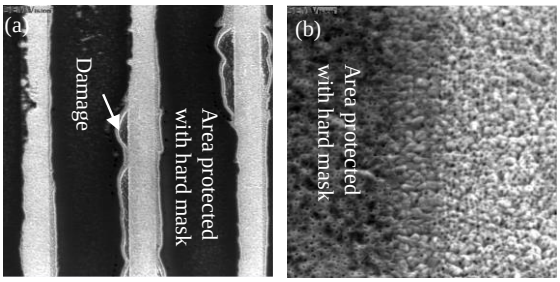

Fig. 4. Role of Al_2O_3 etch process on pattern transfer in SiGe film (a) dry etch (b) wet etch. BCP imprints can be observed in areas protected with Al_2O_3 as well.

4. Conclusions

In this work, we looked at the role of surface roughness on the overall BCP pattern transfer process. An overall reduction in surface roughness either by tuning the deposition process and/or by using a polishing step can improve the patterning process and reduce defectivity. The overall process sequence was seen to have an impact on the final pattern transfer. The results reported here can potentially pave the way for integrating self-assembled BCP for thermal management approaches in semiconductor devices and for performance improvements in MEMS based thermal devices.

5. Acknowledgements:

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