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3D-IC technology in the era of AI, IoT and Big data

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Abstract

3D-IC technology is one of the most important technologies for developing new-generation electronics devices. We present our approach to engineered 3D-IC technology for contributing to the era of AI, IoT and Big data.

1. Introduction

In recent years, with the rapid evolution of AI, IoT and Big data society, performance improvement and energy conservation become a high priority challenge for not only the information and communication devices such as smartphones, tablets, personal computers, and digital home network, but also a wide range of devices such as automobiles, robots, medical devices, and industrial devices. In addition, the cost ratio of semiconductor device to final product has risen sharply due to the increase in development and manufacturing costs of semiconductor devices. Furthermore, a significant reduction in time from R&D to product development to market launch is demanded, as the product cycle of information communication devices such as smartphones has been shortened year by year in order to respond to market needs. As an electronic circuit system integration technology that meets these requirements, system in package (SiP), in which a system is built in a semiconductor LSI package, has attracted extensive attention. Research and development for downsizing, low power consumption, and high functionality are being actively performed around the world, including Japan, the United States, and Europe.

2. 3D-IC technology in electronic circuit integration technology

Moore's law represents a fixed reduction rate in device dimensions. SiP provides the technology called “More than Moore” that realizes integration in the vertical direction. Therefore, it is considered to be complementary for system on chip (SoC) integration method that builds a system on an LSI chip. Furthermore, three-dimensional (3D) integrated technology stacks LSI chips by forming Through-Si-Via (TSV) penetrating through in the LSI chip substrate as shown in Fig.1. It is expected as a technology to achieve various high performances such as ultra-small size with high density, high speed, large capacity, and low power consumption by heterogeneous integration [1]-[6].

3. National project and 3D-IC process prototype line

AIST has been researching and developing the design, analysis and evaluation technologies for 3D integrated packaging system. For the research and development of heterogeneous electronic system using 3D integrated technology, a 3D integrated process prototyping line was established in NEDO's “Next Generation Smart Device Development Project” which is a 5-year project from 2013. This prototype line was built in the TIA-Super Clean Room (SCR) and TIA collaboration center in AIST Tsukuba West Office. This prototype line aimed to build a 3D integrated system development center in cooperation with the conventional design, analysis and evaluation lines. In this project, we researched and developed 3D integrated packaging technology for in-vehicle sensing devices. For reliability research of in-vehicle sensing devices, the development of process technology including TSV at CoC (Chip on Chip) of 3D integrated packaging technology and the research of evaluation technology such as analysis, measurement and inspection of 3D integrated packaging technology were performed as shown in Fig. 2 and Fig. 3 [7]. A 3D integrated system prototype / development center has been established to provide feedback on design, analysis, manufacturing, and evaluation for higher reliability of the 3D

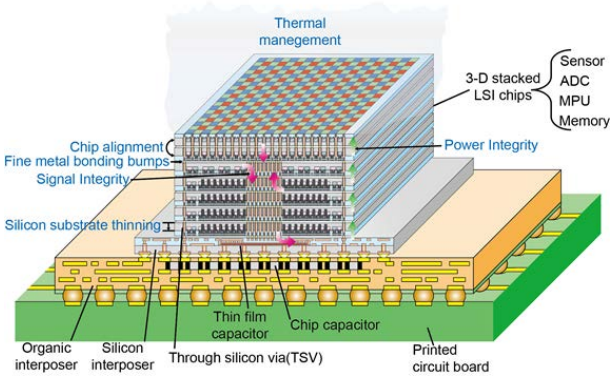

Fig. 1 3D-IC with TSV

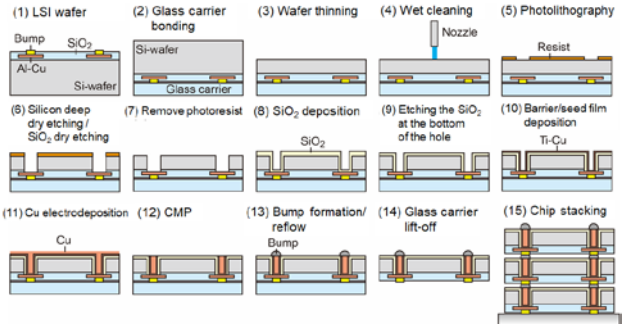

Fig. 2 Process flow for CoC

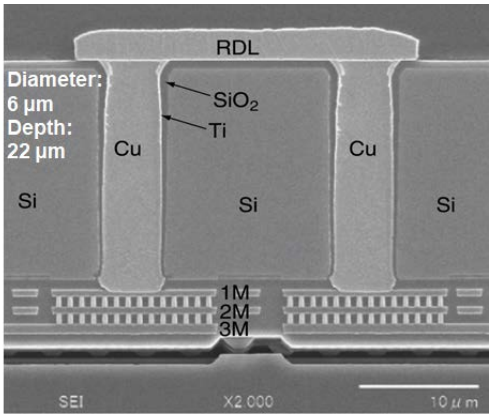

Fig. 3 Cross sectional of the developed TSV.

integrated system.

In addition, from the sensor node at the IoT edge to the IoT gateway and IoT cloud areas, electronic circuits with downsizing, lower power consumption, and higher performance are required. In order to respond to these requirements, the TIA has been working on the research theme "Development of design and manufacturing infrastructure to accelerate IoT technology development" in NEDO's "Open Innovation Pro motion Project for Accelerating IoT Technology Development" for two-year since 2016. Wafer level 3D integrated process equipment for WoW (Wafer on Wafer) process using 300 mm diameter wafers was added into the semiconductor process line in the SCR. Considering collaborating with existing equipment, a 3D integrated process prototype line that can be adopted for the mid-processes and post-processes of semiconductor devices was built as shown in Fig. 4 and Fig. 5 [8]. Combined with the design, analysis, and evaluation technologies of conventional 3D integrated packaging technology, 3D integrated systems are expected to be applied to automotive semiconductor devices and big data processing devices for further development of AI· IoT society. We will

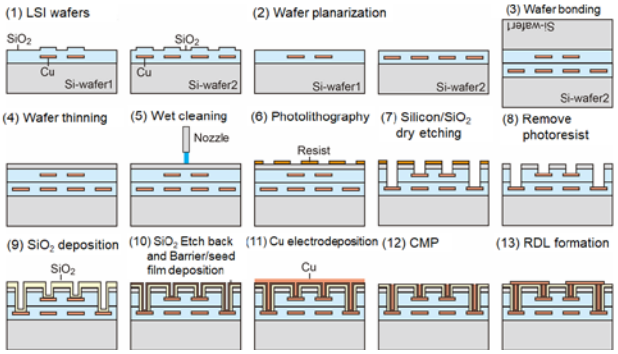

Fig. 4 Process flow for WoW

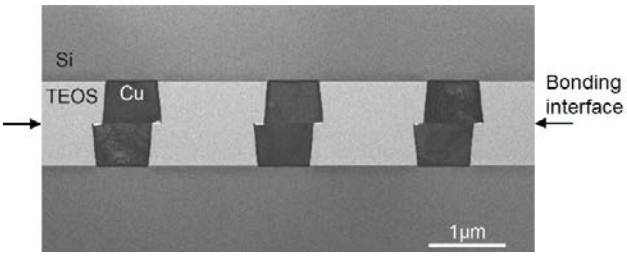

Fig. 5 Cross sectional of bonded wafers with the developed Cu hybrid bonding technology.

contribute importantly to AI· IoT device development in Japanese industries with the research and development toward the realization of heterogeneous 3D integrated systems with low power consumption, high performance.

Acknowledgements

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