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Over 230 fF/μm² capacitance density 9.0V breakdown voltage textured deep trench SiN capacitors toward 3D integration

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Abstract

Si deep trench capacitors with textured surface and SiN dielectric film are presented in this work. The developed capacitors achieved over 230fF/μm² capacitance density, 9.0V breakdown voltage and very low leakage current. The developed capacitors can be utilized for various compact electronic systems using 3D integration.

1. Introduction

Capacitors have been important parts of integrated circuits; small bypass capacitors for LSI, RF/Microwave capacitors, and capacitive elements for analog IC and so on. For compact system integrations, high capacitance density is required. In addition, high reliability such as low leakage current and high breakdown voltage are also required for various applications. Fig. 1(a) shows the correlation between the leakage current density at 1V and the capacitance density of various types of capacitors. Metal-Insulator-Metal (MIM) capacitors and Metal-Insulator-Silicon (MIS) capacitors have low leakage current but relatively low capacitance density of about 50fF/μm² [1-4]. DRAM capacitors have a high capacitance density; however, their leakage current density is targeted to be around 10^{-7}A/cm² [5], thus they are not suitable for analog applications such as sample/hold circuits and amplifiers. Consequently, there is a demand for a capacitor having a high breakdown voltage, a low leakage current, and a high capacitance density, in order to be utilized in various applications. Si trench capacitors with high quality insulator films have been explored for this purpose [6-8]. In addition, for compact system development, these capacitors should be able to be integrated with LSI using 3D integration technologies such as TSV, micro-bumps and hybrid bonding [9]. In this work, we developed versatile high capacitance density and highly reliable Si deep trench capacitors with textured surface and SiN films toward 3D integration. The size of the capacitor can be easily changed as shown in Fig. 1(b).

2. Capacitor design and experimental setup

Eq. (1) shows a simple capacity equation. The capacitance is decided by the surface area, the permittivity of the dielectric, and dielectric thickness. In order to expand the surface area in three dimensions, we introduced textured deep trench with highly reliable SiN as the dielectric.

$$C = \frac{S}{d}\varepsilon \quad (1)$$

Fig. 2 shows layout diagrams of the unit cell. A chip consists of parallel unit cells with deep trench. By choosing the number of connecting unit cells we can select the capacitor area and enhance versatility. In order to suppress warping of wafers during the fabrication process, trench pattern is formed both vertically and horizontally. Fig. 3 shows the process flow of the fabricated wafer and the wafer photograph. Voltage dependency of capacitance is reduced by introducing high doping layer in the substrate. The texture is formed by rugged poly-Si formation [10]. The buried electrode is n^+ doped poly-Si. High temperature process is available with this structure for high reliability. Table I shows the fabricated samples. We verified the influence of trench, dielectric film structures (ONO and NO [11]) and thickness, trench depth, and developed the optimized sample.

3. Results and discussions

Fig. 4 shows measurement results of planar capacitors and trench capacitors (Samples 1, 2). The results show that deep trench enhances about 22 times capacitance with the high breakdown voltage. Fig. 5 shows measurement results of capacitors with different dielectric film structures and thickness (Samples 3, 4, 5). They show that NO structure and thin thickness film lead to high capacitance density and NO structure does not affect breakdown voltage. We decided to use NO structure for high capacitance density and 10 nm thickness for high reliability. Fig. 6 shows the measurement results of breakdown voltage and leakage current density as functions of capacitance density with different trench depths (Samples 6, 7, 8). The result shows no correlation between trench depth and breakdown voltage or leakage current. From the result, we decided to use 14.3μm depth and designed the optimized sample layout (Sample 7'). Fig. 7 shows the TDDB measurement results of capacitors (Sample 7'). Fig. 7(a) shows the Weibull distribution and Fig. 7(b) shows lifetime prediction with a cumulative failure probability of 0.1%, which indicates more than 50 years at 3.3V. Table II shows the performance summary of the developed capacitor. Fig. 8 shows breakdown voltage as a function of capacitance density of various fabricated structures. From the obtained trend, it is expected that the capacitance density will be further improved if the dielectric thickness is reduced for low voltage applications.

4. Conclusions

We developed textured deep trench SiN capacitors over 230fF/μm² capacitance density, 9.0V breakdown voltage and low leakage current. The developed capacitor is based on the versatile design with Si substrate, it can be utilized in various applications through 3D integration for compact systems.

References

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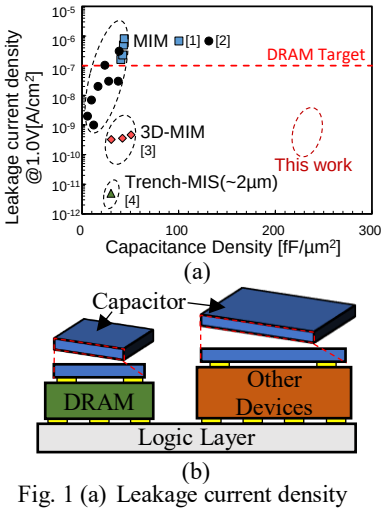


Fig. 1 (a) Leakage current density at 1V as a function of capacitance density, comparing various types of capacitors. (b) Schematic illustration of system integration using stacking with other devices.

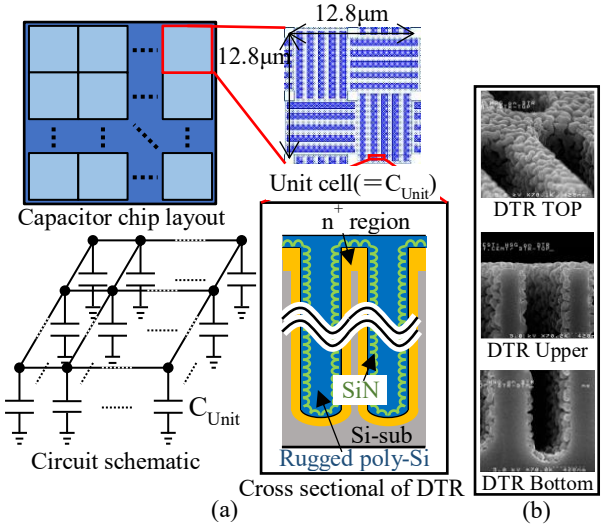


Fig. 2 Structures of a capacitor chip. (a)Layout diagrams of the unit cell with deep trench (DTR). Circuit schematic representing parallel unit cells. (b)SEM view of the fabricated textured deep trench.

8' (100) N-type Cz/5.0-8.0Ωcm

- Si deep trench formation
- n^+ Si formation
- Rugged poly-Si deposition
- Dielectric film formation
- Doped poly-Si electrode formation
- Inter-metal dielectric film formation
- Contact formation
- Metallization (3 Metal)
- Passivation film formation, PAD opening

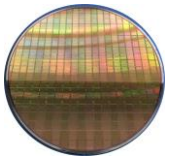


Fig. 3 Process flow and wafer photograph.

Table I. Summary of the fabricated samples.

Sample No.	Trench	Dielectric film structure	Dielectric thickness[nm]	Trench depth[μm]
1	X	ONO	13.8	12
2	O			
3	O	ONO	13.8	12
4			9.0	
5		NO	9.0	
6	O	NO	10	16.2
7				14.3
8				11.7

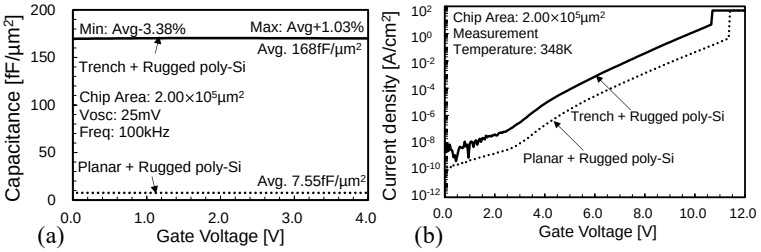


Fig. 4 Measurement results of planar and trench capacitors (Samples 1, 2). (a) CV characteristics showing 22 times higher capacitance density with deep trench compared to planar structure. (b) IV characteristics showing enough high breakdown voltage with deep trench.

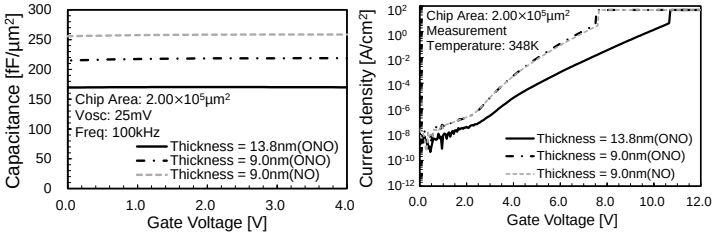


Fig. 5 Measurement results of capacitors with different dielectric film structures and thickness (Samples 3, 4, 5). (a) CV characteristics showing NO structure and thin thickness film lead to high capacitance density. (b) IV characteristics, showing NO structure does not affect breakdown voltage.

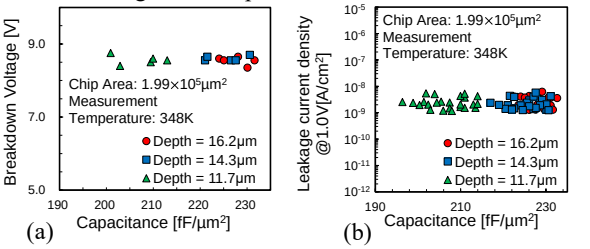
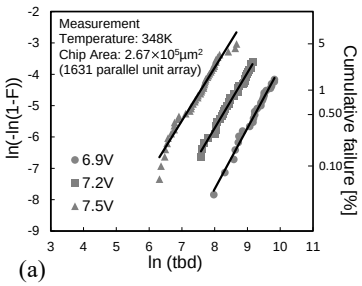


Fig. 6 (a)Breakdown voltage as a function of capacitance density. (b) Leakage current density at 1V as a function of capacitance density (Samples 6, 7, 8) The results show no correlation between trench depth and breakdown voltage or leakage current.



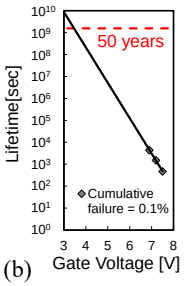


Fig. 7 TDDB measurement results of the developed capacitors (Sample 7'). (a) Weibull distribution. (b) Lifetime prediction with a cumulative failure probability of 0.1%.

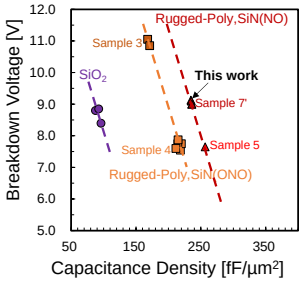


Fig. 8 Comparison of breakdown voltage as a function of capacitance density among various fabricated structures.

Table II. Performance summary of the developed capacitor.

Technology	Deep trench + Rugged poly-Si + Unit cell structure
Area of unit cell	12.8μm x 12.8μm
Dielectric film structure /thickness	NO/10nm
Trench depth	14.3μm
Capacitance	235fF/μm²
Breakdown voltage	9.0V
Leakage current density(at 1V)	Below 10^{-8}A/cm²
TDDB lifetime(at 3.3V)	Over 50 years