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Effect of Dielectric Layer Scheme for High-Quality Silicon Channel in Monolithic 3DIC

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Abstract

In this study, the quality of silicon channel fabricated by cooling hole structures is investigated, including different structures and kinds of dielectric layers. The discontinuous dielectric layer of Si_3N_4 can assist to provide high-quality silicon channel due to the induced thermal stress. Based on the high-quality result of silicon channel, location-controlled-grain technique with a discontinuous layer of Si_3N_4 could be a feasible technology and scheme to achieve high performance monolithic 3D integration circuits.

1. Introduction

Monolithic 3D integration can provide a promising solution to enhance system functionality, decrease power consumption, boost inter-layer connectivity and minimize chip dimension, as shown in Figure 1 [1]. Direct fabrication of 3D stackable channel using low thermal budget laser crystallization is one of the promising methods to realize monolithic 3D FinFET circuits [2-3]. However, variations on both I_{on} and I_{off} [4-5] are greatly increased when FinFETs are fabricated on grain boundaries, which are induced by the polycrystalline process. In view of these, a location-controlled-grain technique has been proposed for monolithic 3D FinFET fabrication to improve the system performance [6].

In this study, several structures and kinds of dielectric layer to improve the crystallinity of the Si layer above SiO_2 are investigated. To further understand the effectiveness of this improvement, BEOL FinFETs were fabricated using this scheme.

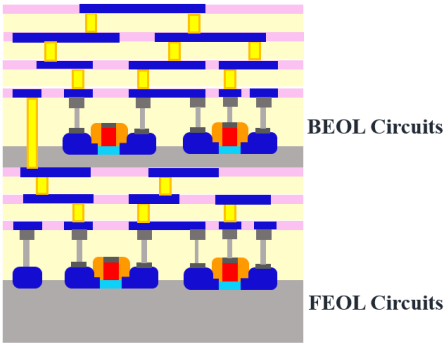

Fig. 1 The illustration of Monolithic 3DIC

2. Experimental Methods

2.1. Sample Fabrication

Figure 2 shows the process flow of the sample fabrication with the location-controlled-grain (LCG) technique. At first, 500 nm SiO_2 was deposited on an 8-inch Si wafer. Then, several kinds of dielectric layer such as 10 nm Si_3N_4, 3 nm Al_2O_3 and 3 nm HfO_2 were deposited on SiO_2 successively and respectively. The cooling hole structure as shown in Figure 3 was formed by etching into 200 nm in SiO_2 layer. Next, conformal 100 nm amorphous silicon (a-Si) deposition and green nanosecond pulse laser were both applied to improve the quality of the film. Lastly, secco etching was used to locate the position of grain boundary.

2.2. Cooling hole structure

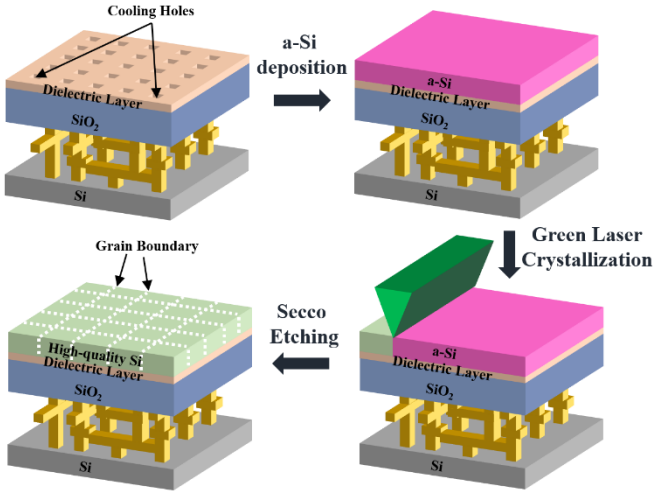

Fig. 2 Process flow of sample fabrication with location-controlled-grain technique

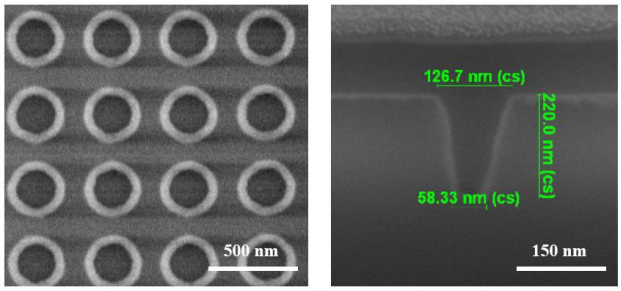

Fig. 3 SEM image of cooling hole structure (a) top view (b) cross section view

With a controlled pumping laser power density, the vast majority of the a-Si layer can reach their melting point except for the bottom of the cooling hole. Therefore, un-melted a-Si in the bottom of the cooling hole would act as nucleation

seeds which will initiate vertical growth, and there would be only one grain "selected" during crystallization.

3. Results and Discussion

In the beginning, the a-Si was deposited only on SiO_2 layer. However, the quality as shown in Figure 4 has many intra-grain defects. In order to improve the grain quality, different structures with several kinds of dielectric layer such as Si_3N_4, Al_2O_3, and HfO_2 are investigated and shown in Figure 5 and Figure 6.

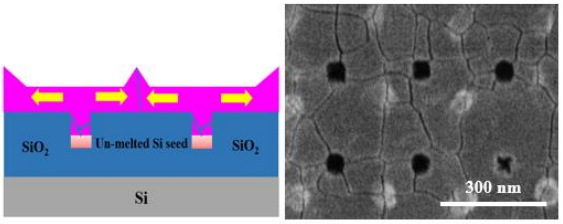

Fig. 4 The illustration and SEM image of location-controlled-grain with only SiO_2 layer

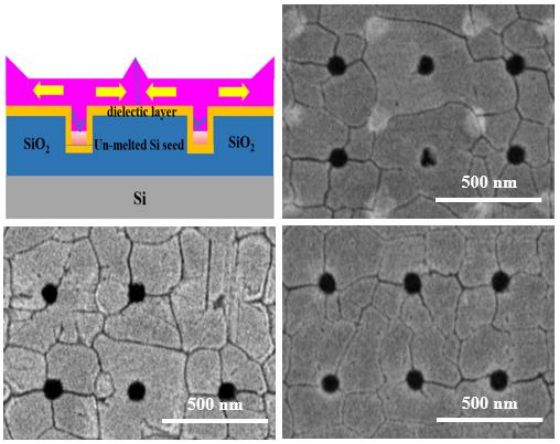

Fig. 5 The illustration and SEM image of location-controlled-grain with continuous dielectric layer (a) Si_3N_4 (b) Al_2O_3 (c) HfO_2

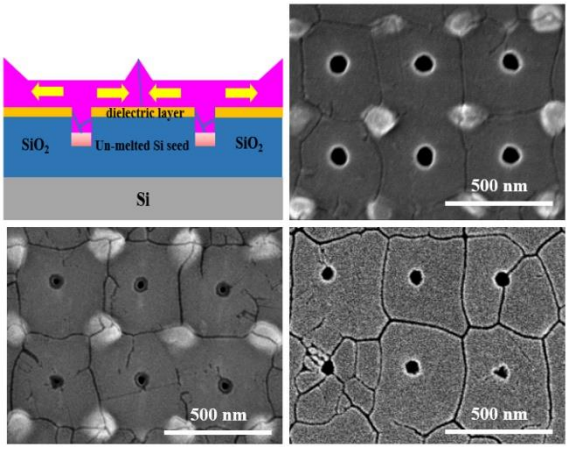

Fig. 6 The illustration and SEM image of location-controlled-grain with discontinuous dielectric layer (a) Si_3N_4 (b) Al_2O_3 (c) HfO_2

It can be clearly observed that the discontinuous dielectric layer has the better quality than that of the continuous dielectric layer. This is because that particles could be deposited inside the cooling hole for the continuous dielectric layer, and these particles can be treated as additional nucleation sites to deteriorate the crystallinity of the Si layer.

In addition, it is obvious that Si_3N_4 has the better crystallization compared with Al_2O_3 and HfO_2. Though the proper compressive stress can reduce the nucleation sites due to the mismatch of coefficient of thermal expansion [7], the too large compressive stress induced by the Al_2O_3 and HfO_2 still can damage the film quality.

To understand the effectiveness of this LCG technique with Si_3N_4 layer, BEOL FinFETs were fabricated by the high-quality Si film, and the electrical properties were compared with random grains as shown in Figure 7. It is evident that the LCG technique with Si_3N_4 layer provides FinFETs with better S.S., I_{on} and I_{off}.

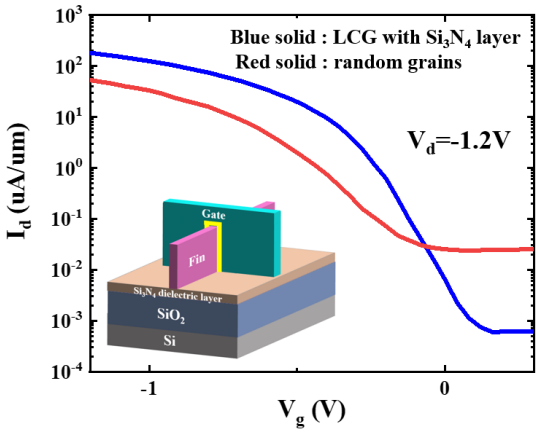

Fig. 7 The comparison of I_d-V_g of FinFET fabricated by high-quality silicon channel and random grains

Conclusions

In this paper, LCG technique has been successfully demonstrated. By using the cooling hole structure with the discontinuous dielectric layer of Si_3N_4, high-quality silicon channel was obtained and the electrical properties of FinFETs fabricated with this scheme were further improved. Thus, this improved scheme can provide a high-quality silicon channel and accordingly realize monolithic 3DIC.

Acknowledgements

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