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Circuit Technology for High-speed Wireline Communication

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Abstract

Wireline transceivers that realize inter-processor communications at high data rate are required to improve computation performance. To achieve the required data rate, wireline transceivers were designed with circuits to enhance the bandwidth (BW). In this paper, we introduce the high-speed electrical and optical transceivers and circuit technologies we developed to realize signal transmission at tens of gigabits per second.

1. Introduction

With the rapid growth of data traffic in data centers, higher data transfer rates are required for inter-processor communications as shown in Fig. 1. In large-scale computer systems, the workload is executed using multiple processors in parallel. Improving computation performance requires not only advancements in processing power, but also advancements in input/output (I/O) bandwidth (BW).

In this paper, we introduce 56Gb/s electrical and 25Gb/s optical transceivers and circuit technologies we developed to achieve the required I/O BW. In addition, we introduce the latest circuit technologies for achieving 100Gb/s.

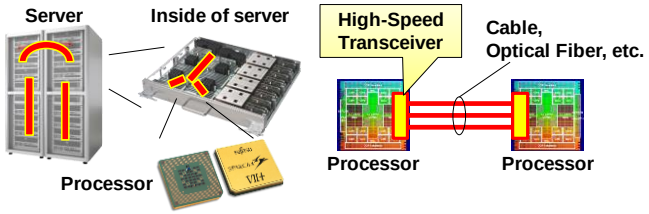

Fig. 1 High-speed wireline transceivers

2. 56Gb/s Electrical Transceiver

A block diagram of the 28nm CMOS transceiver [1] is shown in Fig. 2. This transceiver has a two-lane configuration, with each lane supporting 56Gb/s non-return-to-zero (NRZ) signal transfer. The transmitter (TX) converts 1.75Gb/s 32-bit signals, corresponding to the signals from a processor core circuit, into a 56Gb/s signal using multiplexers (MUXs). The receiver (RX) converts a 56Gb/s signal into 1.75Gb/s 32-bit signals using demultiplexers (DMXs).

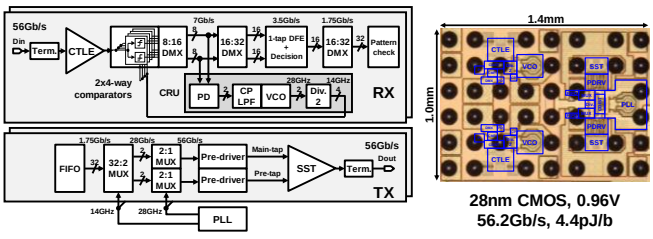

Fig. 2 56Gb/s transceiver block diagram and chip micrograph

The TX front-end circuit is shown in Fig. 3(a). The output stage is a source-series-terminated (SST) driver that has a capacitor connected in parallel with the series-termination resistor to improve eye opening [2]. The 2-tap feed-forward equalizer (FFE) to compensate for the frequency-dependent signal loss in the transmission media is implemented by connecting the outputs of the two SST drivers corresponding to the main-tap and pre-tap in Fig. 2.

The RX front end has a continuous-time linear equalizer (CTLE), as shown in Fig. 3(b). The CTLE also compensates for the signal loss and consists of a high-frequency equalizer (HFEQ) and a low-frequency equalizer (LFEQ) [3]. The HFEQ is a single-stage source-degenerated amplifier, and the LFEQ is a two-stage equalizer with a feedback circuit that generates an additional zero at a low frequency.

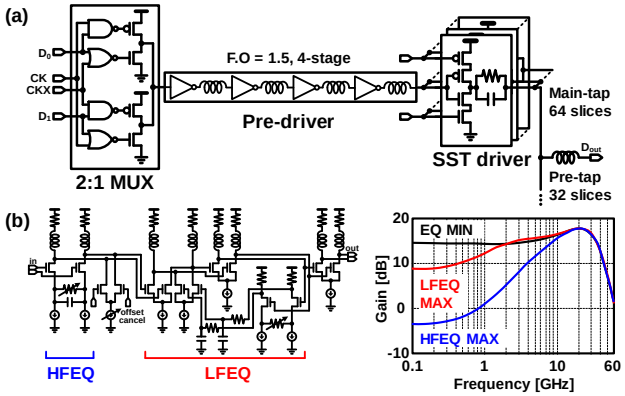

Fig. 3 (a) TX 2-to-1 MUX and SST driver stage, (b) RX CTLE

The clock-recovery unit (CRU) in the RX adjusts the sampling phase to sample the CTLE output signal. Our scheme requires eight comparators and a four-phase quarter rate clock to perform phase detection as shown in Fig. 2. We explain the scheme using a simplified model in Fig. 4 to make understanding the operating principle easier. The plot on the right shows a simulated eye at the comparator input. The red, blue, and green dashed lines correspond to the high-threshold level, low-threshold level, and sampling phase of the comparator, respectively. The phase of the data is measured when the sequence is either 011 or 100. For example, when 011 is detected, the output of the high-threshold level comparator for the center bit is used to determine whether the timing is early or late. The output of the low-threshold level comparator is used for data decision. The operation of this scheme also includes a one-tap speculative decision-feedback equalizer (DFE) to compensate for signal loss. The threshold level of the comparator corresponds to the tap coefficient. The conventional scheme has separate comparators for phase detection and DFE. In contrast, our

proposed scheme uses the same comparators for phase detection and DFE, and reduces the power consumption as a result by reducing the number of comparators.

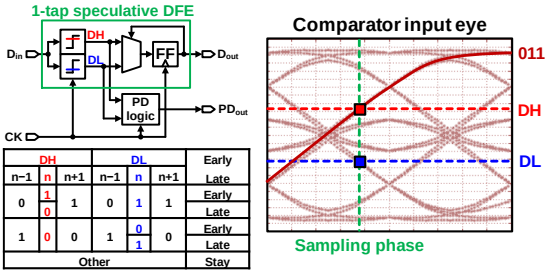

Fig. 4 Phase detection and data decision

The 56.2Gb/s TX output eye observed through a channel loss of 7.2dB at 28.1GHz is shown in Fig. 5(a). The RX jitter tolerance curve in Fig. 5(b) measured using a 56.2Gb/s at BER=10^{-12} satisfies the OIF CEI-56G-VSR MASK. The transceiver achieved 18.4dB loss compensation at 56.2Gb/s.

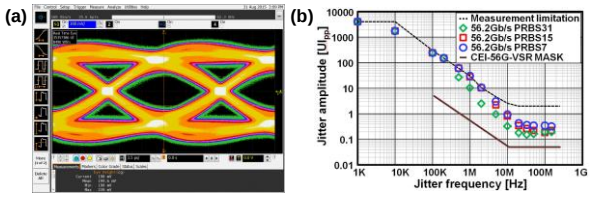

Fig. 5 (a) TX eye diagram (PRBS15), (b) RX jitter tolerance

3. Hybrid Integrated Silicon Photonic (SiPh) Transceiver

Integrated photonic interconnect technology does not suffer from the bandwidth-distance limitation intrinsic to electrical interconnects, and promises to be a disruptive alternative for next-generation scalable data centers. We developed a hybrid integrated SiPh transceiver with an electrical-optical interface that includes a 28nm CMOS driver/TIA chip and a SOI modulator/PD chip [4] shown in Fig. 6.

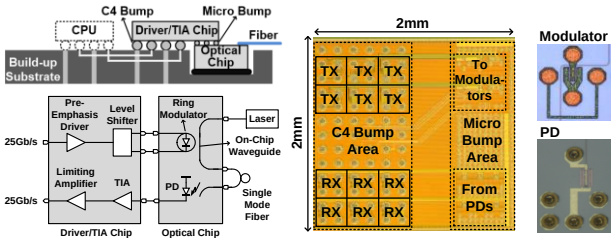

Fig. 6 Transceiver structure, block diagram, chip micrograph

A pseudo-differential driver and a 2-tap FIR filter with a tap delay of 0.5UI and coefficient of 0.8 enable an 800MHz BW carrier-injection ring modulator to be operated at 25Gb/s. The TIA implements two BW-enhancement techniques as shown in Fig. 7, namely, a regulated-cascode input stage with shunt-shunt feedback and T-coil inductive peaking and a hybrid offset calibration, achieving 25Gb/s.

In the TX measurement, a 1550nm laser source is used to generate an optical signal, and the modulated optical signal is observed by an oscilloscope. The RX output electrical eye and BER versus PD input optical modulation amplitude (OMA) are shown in Fig. 8. A BER of 10^{-12} is achieved with -8.0dBm OMA.

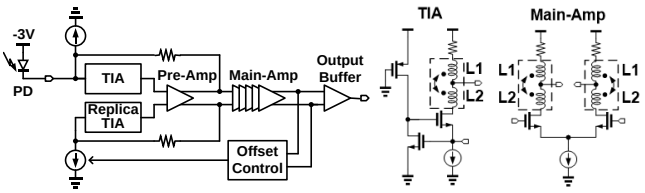

Fig. 7 RX schematic for SiPh transceiver

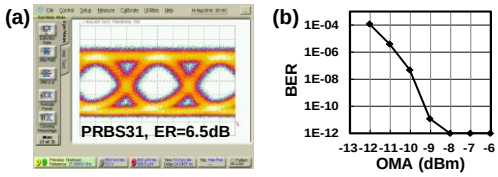

Fig. 8 (a) 25Gb/s TX optical output, (b) RX sensitivity

4. Circuit technology to achieve 100Gb/s or more

Four-level pulse amplitude modulation (PAM4) has become the dominant scheme for 100Gb/s because 2 bits can be transmitted simultaneously through multiplexing in the amplitude direction. Therefore, PAM4 has better spectral efficiency than NRZ. However, because the signal amplitude of PAM4 is only 1/3 that of NRZ, the signal quality is likely to be degraded by the PVT variations of the analog front-end circuits, such as the TX driver and RX CTLE. Compensation for these variations is thus necessary. In addition, the number of FFE and DFE taps need to be adjustable to accommodate various transmission media and lengths. The suitability of digital circuits for adaptive control has led to the ongoing development of digital-to-analog converter (DAC)- and analog-to-digital converter (ADC)-based transceivers using digital signal processing (DSP) [5,6,7] to meet these requirements, as shown in Fig. 9.

In the future, high-speed and low-power DACs and ADCs, and architectures that simplify digital signal processing will become key technologies.

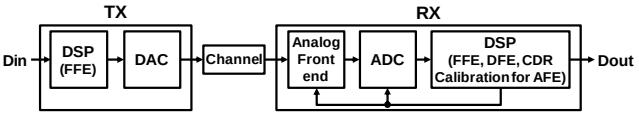

Fig. 9 DAC- and ADC-based transceiver using DSP

5. Conclusions

In this paper, we introduced high-speed wireline transceivers and circuit technologies that achieve the desired data rate by compensating for the signal loss. DAC- and ADC-based transceivers using DSPs have become the dominant architecture for data rates above 100Gb/s. The continued improvement of data rates will be realized by digital signal processing together with BW enhancement using the analog front-end circuits introduced in this paper.

References

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