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PdErSi Source and Drain for Schottky Barrier MOSFET with HfO_2 Gate Insulator Fabricated by Low Thermal Budget Gate-First Process

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Abstract

We investigated the integration of the novel alloy PdErSi as source and drain (S/D) regions in gate-first p-channel Schottky barrier (SB) MOSFET. The low thermal budget process of 500°C/1 min formed the highly-oriented PdErSi($11\bar{2}0$) hexagonal crystal structure. Furthermore, the gate-first SB p-MOSFETs with PdErSi S/D regions were realized for the first time. The hole mobility of 46.4 cm^2 $V^{-1}s^{-1}$ was obtained.

1. Introduction

The metal silicides are required in gate-first Schottky barrier (SB) MOSFET because of its low-thermal budget process for the source and drain (S/D) formation and its precise gate length scaling [1]. Dual silicides such as ytterbium silicide ($YbSi_{2-x}$) for nMOSFET and platinum silicide (PtSi) for pMOSFET are used as S/D regions in SB MOSFETs [2, 3]. However, the formation of the $YbSi_{2-x}$ or PtSi S/D regions are usually performed at 600°C or above. In this regard, the high-k gate insulators such as HfO_2 require low thermal budget process below 600°C. Since a single silicide material is preferred for both nMOSFET and pMOSFET, the PdErSi with work function near the Si midgap would be ideal as a S/D region with Schottky barrier height (SBH) control by dopant segregation (DS) process [4-7].

Previously, the low contact resistivity of 4.8×10^{-8} Ω-cm^2 on PdErSi/n^+-Si(100)/p-Si(100) contacts with phosphorus (P^+) DS process was achieved [4]. The silicidation and DS process were performed for as low as 500°C/5 min.

In this research, the PdErSi/Si(100) contacts were integrated as S/D regions in the gate-first SB pMOSFET for the first time. The SB pMOSFETs were realized using the low thermal budget process.

2. Experimental Procedure

Figure 1 shows fabrication of the gate-first SB p-channel MOSFET (pMOS) [6]. The HfO_2 formed with low temperature process of 600°C was used as a gate insulator [8]. The n-Si(100) substrates (1-10 Ω-cm) were cleaned using SPM (H_2SO_4:H_2O_2 = 4:1) and DHF (HF:H_2O, 1% HF). Next, 180-nm-thick SiO_2 field oxide (FOX) was formed using wet oxidation at 850°C. Then, the active regions and the channel stop (CS) regions were formed. Next, the 20-nm-thick HfO_2 gate stack was deposited using RF magnetron sputtering at room temperature (RT). A 3-inch Hf target was utilized for the HfO_2 reactive sputtering with 2.0/0.2 sccm Kr/O_2 and 60 W RF power. The 20-nm-thick PdEr metal was in-situ formed after

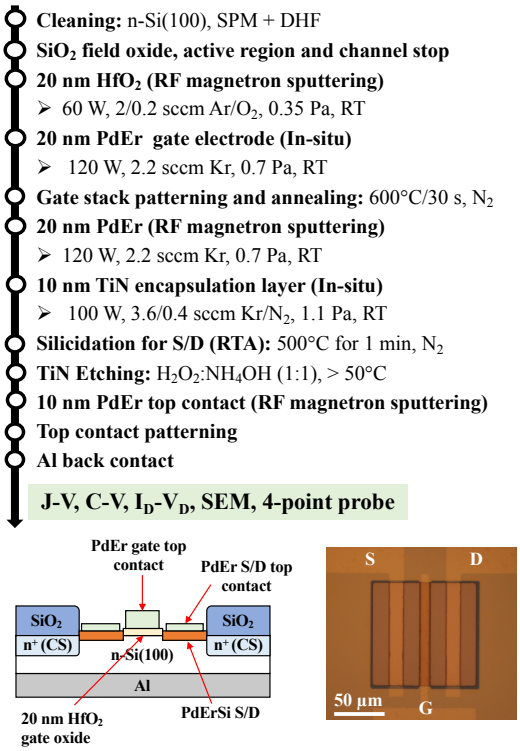

Figure 1 The fabrication process, schematic cross-section and the plane view image of the gate-first SB MOSFET.

the HfO_2 formation. The developed PdEr (3:2) metal target was utilized in the metal gate deposition with 2.2 sccm Kr and 120 W RF power at RT. The deposition pressure is 0.7 Pa. Then, the PdEr/HfO_2 gate was patterned and etched. A two-step etching process was used to form the metal gate. The first step is the diluted aqua regia (HCl:HNO_3:H_2O, 3:1:10) etching for 4-5 s at 45°C. The second step is the HNO_3 etching for 2 s at the same solution temperature of 45°C. The HfO_2 was etched in DHF for 25 s. Then, the PdEr/HfO_2 gate stack structure was annealed in RTA at 600°C/30 s in N_2 ambient. The sample was dipped in DHF for 10 s to etch the unintentional oxide before the formation of the TiN/PdEr layer for the S/D regions. The 20-nm-thick PdEr film was deposited next. The deposition condition is the same as the PdEr metal gate formation. The 10-nm-thick TiN encapsulation was in-situ formed with 100 W RF power, 3.6/0.4 sccm Kr/N_2 and 1.1 Pa pressure utilizing TiN target. The silicidation annealing was carried out using RTA at 500°C/1 min under N_2 ambient. After the silicide S/D formation, the TiN encapsulation layer was etched by NH_4OH:H_2O_2 (1:1) solution at 50°C. Then, the 10-nm-thick PdEr top contact was formed. The

PdEr top contacts were patterned and formed by the two-step etching process. Finally, the Al back contact was formed by resistive evaporation. The x-ray diffraction (XRD), scanning electron microscopy (SEM), C-V, J-V, and I_D-V_D measurements were performed.

3. Results and Discussion

Figure 2 shows the XRD patterns of the PdEr film and the PdErSi [7]. The PdErSi(11$\bar{2}$0) peak with hexagonal crystal structure was formed from the amorphous PdEr film with low temperature annealing of 500°C/1 min. The peak is located at 27.37° with lattice spacing of 3.256 Å. Compared with the Pd_2Si that has lattice spacing of 3.248 Å, the larger lattice spacing of PdErSi must be due to the replacement of the Pd atoms by Er atoms with larger covalent radius. The inset shows that the PdErSi has smooth surface morphology after the etching process. The resistivity of the PdErSi film is 161 μΩ-cm obtained from the 4-point probe data.

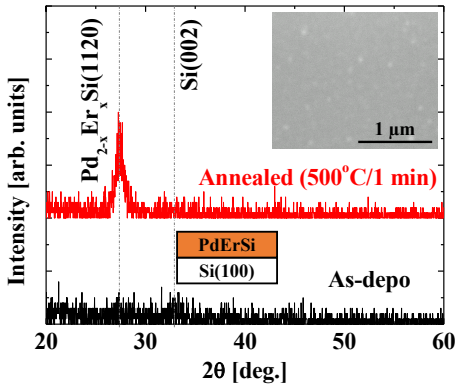

Figure 2 XRD characteristics of PdErSi and PdEr films.

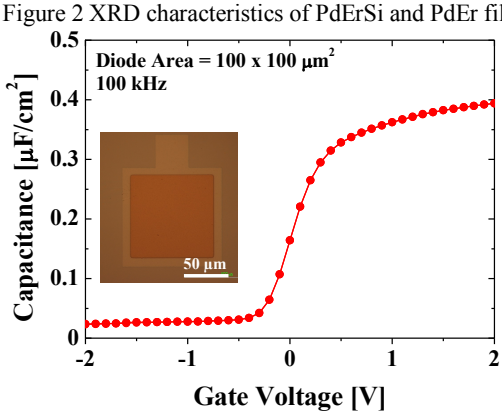

Figure 3 C-V characteristics of the PdEr/HfO_2/n-Si(100) gate stack structure.

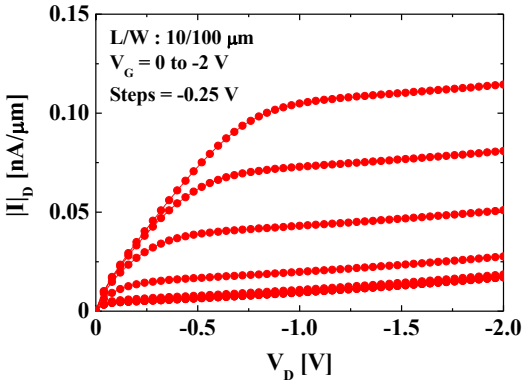

Figure 4 I_D-V_D characteristics of the SB pMOSFET with L/W of 10/100 μm.

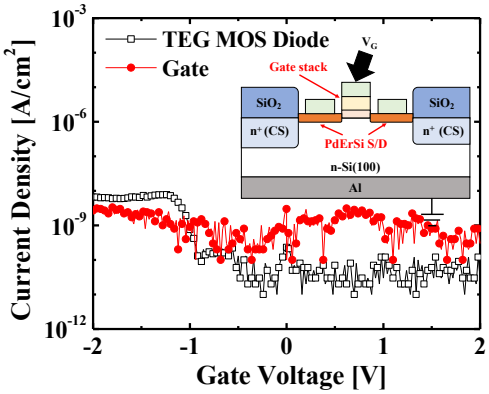

Figure 5 J-V characteristics of the TEG MOS diode and the gate stack.

Figure 3 shows the C-V of the PdEr/HfO_2/n-Si(100) gate stack structure. By utilizing the in-situ process in the gate stack formation, the interface properties were improved as shown by the zero hysteresis width. By utilizing the Terman method, the density of interface states (D_{it}) of 7.7×10^{10} cm^{-2} eV^{-1} was obtained. The PdEr metal contact has a work function (ϕ_m) of 4.81 eV and the HfO_2 gate insulator has an equivalent oxide thickness (EOT) of 8.5 nm. The relative dielectric constant (ε_r) of 8.9 was also obtained.

Figure 4 shows the I_D-V_D characteristics of the SB pMOSFET device with L/W of 10/100 μm. From the I_D-V_G characteristics (not shown), the linear hole mobility (μ_{lin}) of 46.4 cm^2 $V^{-1}s^{-1}$ and threshold voltage (V_{TH}) of -1.08 V were obtained. From the J-V measurements, the PdErSi/n-Si(100) contacts in the S/D regions have SBH for hole of 0.41 eV. The gate J-V has leakage current density of 2.7×10^{-9} A/cm^2 which is comparable to the test element group (TEG) diode's leakage current density of 6.7×10^{-9} A/cm^2 in Fig. 5 which shows that the insulating property of HfO_2 was maintained.

4. Conclusions

The PdErSi/Si(100) contacts were formed utilizing the low thermal budget process as S/D in gate-first SB MOSFETs with HfO_2 gate insulator for the first time. Therefore, the PdErSi is an attractive material for the low temperature integration of the high-k gate stacks in the gate-first MOSFETs.

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