Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp181-182

The Si-terminated 2DHG Diamond MOSFETs with Normally-off Operation and Wide temperature Stability (~673 K)

Yuta Nameki[1], Bi Te[1], Wenxi Fei [1], Jun Tsunoda[1], Naoya Niikura[1], Atsushi Hiraiwa[1,3] and Hiroshi Kawarada[1, 2]

[1] School of Advanced Science and Engineering Waseda Univ.
3-4-1 Okubo, Shinjuku-ku, Tokyo 169-8555, Japan
Phone:+81-3-5286-3391 E-mail: yuta_n-1225@toki.waseda.jp
[2]The Kagami Memorial Laboratry for Material Science and Technology
2-8-26 Nishiwaseda, Shinjuku-ku, Tokyo 169-0051, Japan
[3] Institute of Materials and Systems for Sustainability (Tokyo Branch), Nagoya University

Abstract

We fabricated Si-terminated (C-Si) diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) for the first time. At room temperature, the maximum drain current density of the C-Si diamond MOSFET normalized by gate width is -114 mA/mm at V_{DS} of -30V and V_{GS} of -40V, and the peak transconductance is 2.3 S/mm at the V_{DS} of -30V. The field effect mobility (μ_{EF}) is 106 $cm^2V^{-1}s^{-1}$. In addition, the Si-terminated MOSFET shows the normally off operation with threshold voltage V_{th} = -5.0 V. Then, we confirmed the temperature stability in a wide temperature range (up to 673 K). This value is considered to have a potential comparable to that of C-H diamond MOSFETs.

1. Introduction

Diamond is the next generation wide bandgap semiconductor material, which can realize high performance power devices. The electrical properties of diamond are affected by the surface modification. The H-terminated (C-H) diamond has low activation energy, high carrier mobility [1] and high hole density. We have developed the C-H diamond MOSFETs by using the two-dimensional hole gas (2DHG), and reported high drain current output [2], wide high temperature operation [3], and high breakdown voltage [4] by using the atomic layer deposition (ALD) method -Al_2O_3 as the gate insulator. In this time, we propose a silicon-terminated (C-Si) structure using SiO_2 to achieve further diamond device development. We consider SiO_2 is advantageous for power devices in terms of chemical stability and wide bandgap. The SiO_2 can be used as the gate insulator in the diamond power device application and we can fabricate MOSFETs by using the C-Si diamond as the p-channel. it is considered C-Si bonding on the diamond-SiO_2 interface can reduce the interface state and improve the hole mobility. In this work, we fabricated C-Si diamond MOSFETs with the B-doped diamond selective growth using the SiO_2 as the mask for source and drain formation and the gate insulator for the first time. As a result, C-Si diamond MOSFETs achieved normally-off operations [5]. Furthermore, we have investigated channel mobility and wide temperature stability.

2. Device Fabrication

The cross-sectional image of the C-Si diamond MOSFET is shown in Fig.1 (a). And, Fig.1 (b) shows an optical micrograph of the C-Si diamond MOSFET. The device fabrication method is as follows. The undoped diamond layer of thickness 2 μm was grown on the Ib (100) diamond substrate via microwave plasma chemical vapor deposition (MPCVD). The power of the microwave plasma was 750 W, and the chamber pressure and temperature during growth were 35 Torr and 600 ºC, respectively. After surface cleaning by acid treatment, the diamond surface was oxidized by UV-ozone. The 260 nm SiO_2 layer was formed on Ib (100) substrate by utilizing TEOS-CVD. The source and drain patterns were etched using the inductive coupled plasma reactive ion etching (ICP-RIE). After that, the 130 nm B-dope diamond layer was selectively grown on the etched patterns using SiO2 mask by MPCVD. The growth temperature and microwave output power of MPCVD were 727 °C and 360 W, respectively. In this process, the C-Si bonding has been formed during 130 nm selective growth of B-doped (~10^{21} cm^{-3}) diamond film. Metal electrodes (Ti/Pt/Au) were formed on the surface of the selected B-doped diamond. Ohmic contacts were formed by annealing. The SiO2 film except the channel was removed by ICP-RIE. The 100 nm Al_2O_3 was deposited as a gate insulating on the diamond substrate using the ALD method at 450 °C. Finally, a 100 nm gate with 2 μm overlapping to the source-drain electrode was evaporated. The gate width, gate length, source-drain length and length of SiO_2 were 25, 20, 16, and 6 μm, respectively.

3. Results and Discussion

An enlarged view of the SiO_2/diamond interface is shown in Fig.2 (a). C-Si bonding are formed at the interface between SiO_2 and diamond. During selective epitaxial growth of diamond through SiO2 masks, Si-terminated were formed on diamond surface by replacing oxygen terminations under the masks. The high temperature of selective growth and its reductive atmosphere allowed Si atoms in SiO_2 to interact with diamond surface. Thus, C-Si diamond composed of monolayer or thin multilayers of carbon and silicon bonds on diamond. Fig.2 (b) showed

XPS analyses of the diamond/SiO_2 interface. The components related to C-Si are clearly recognized in the C1s x-ray photoelectron spectroscopy XPS spectrum. As a result, C-Si bond at the banding energy of 284.22 eV and 282.84eV was confirmed.

Fig.3 showed I_{DS}-V_{DS} characteristics from room temperature (RT) to 673 K. These devices have 25 μm gate width (W_G) and 6 μm source-drain length (L_{SD}). At RT, the maximum drain current density of the C-Si diamond MOSFET normalized by gate width was -114 mA/mm at V_{DS} of -30V and V_{GS} of -40V. And, the peak transconductance was 2.5 mS/mm. Regarding the temperature characteristics from 373K to 673K, the maximum drain current densities were -110, -153, -80 and -112 mA/mm at V_{DS} of -30V and V_{GS} of -40V, and the peak transconductance was 2.2, 2.9, 2.6 and 2.9 mS/mm at the V_{DS} of -30V, respectively. These results show that stable drain current characteristics and transconductance are obtained even at high temperature. In addition, the field effect mobility (μ_{EF}) from RT to 673 K were 106, 114, 135, 118 and 133 $cm^2V^{-1}s^{-1}$, respectively. These values are considered to have a potential comparable to that of C-H diamond MOSFET.

Fig.4 showed I_{DS}-V_{GS} characteristics from room temperature (RT) to 673 K with V_G from -30V up to 25V and V_{DS} of -10V. The threshold voltages of the Si-terminated MOSFET were -5.0, -2.4, -5.0, -7.1 and 4.8 V, respectively. These characteristics showed normally-off operation in a wide temperature range.

The normally-off operation using this C-Si diamond with $SiO_2$is expected to develop as a new normally-off method for diamond devices. Moreover, the temperature stability of the C-Si diamond MOSFET was confirmed. These results suggest that the C-Si diamond MOSFET method can be applied to vertical-type diamond devices. It also makes a significant contribution to diamond p-FETs in high voltage CMOS circuits combined with GaN or SiC n-FETs.

4. Conclusion

We fabricated Si-terminated diamond metal-oxide-semiconductor field-effect transistors (MOSFETs). The maximum drain current density of the C-Si diamond MOSFET, the peak transconductance and the field effect mobility (μ_{EF}) are considered to have a potential comparable to that of C-H diamond MOSFETs. In addition, the Si-terminated MOSFET shows the normally off operation with threshold voltage V_{th} = -5.0 V. The normally-off operation using this Furthermore, we evaluate the temperature characteristics from 300 to 673K, and confirm the temperature stability. It will contribute significantly to the diamond p-FET for high voltage CMOS circuits combined with GaN or SiC n-FETs.

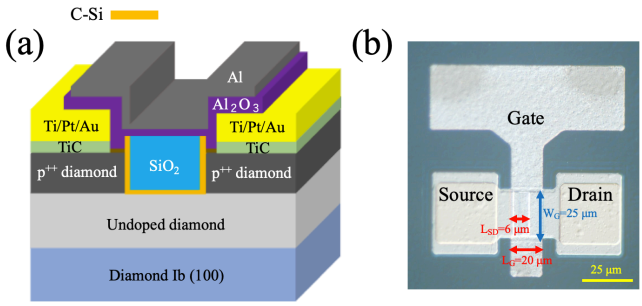

Fig.1 (a) Cross-sectional image of the Si-terminated diamond MOSFET. (b) An optical micrograph of the Si-terminated diamond MOSFET.

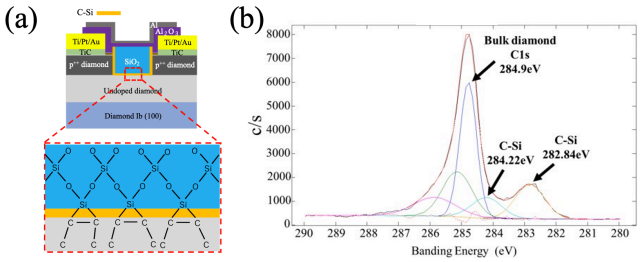

Fig.2 (a) An enlarged view of the SiO_2/diamond interface. C-Si bonding are formed at the interface between SiO_2 and diamond. (b) XPS analyses of the diamond/SiO2 interface [5].

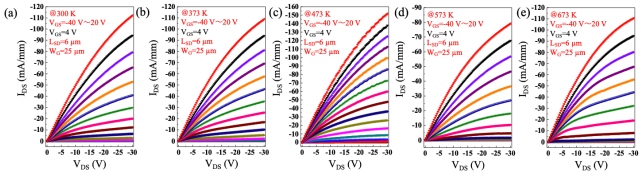

Fig.3 I_{DS}-V_{DS} characteristics. From RT to 673 K, the maximum drain current densities of the C-Si diamond MOSFET normalized by gate width were -114, -110, -153, -80, and -112 mA/mm at V_{DS} of -30V and V_{GS} of -40V, respectively. (W_G = 25 μm, L_{SD} = 6 μm)

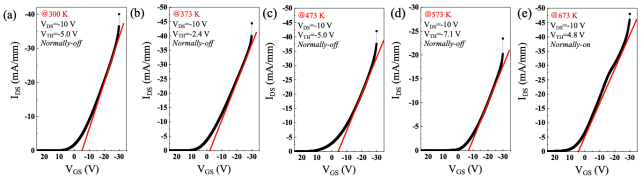

Fig. 4 I_{DS}-V_{GS} characteristics from RT to 673 K with V_G from -30V up to 25V and V_{DS} of -10V. The threshold voltages of the Si-terminated MOSFET were -5.0, -2.4, -5.0, -7.1 and 4.8 V, respectively. (W_G = 25 μm, L_{SD} = 6 μm)

Acknowledgements

This study was partially supported by Creation of Life Innovation Materials for Interdisciplinary and International Researcher Development.

References

[1] Y.Sasama, T.Yamaguchi, et al.,APL Mater. 6(2018)

[2] K.Hirama, M.Kasu, et al., Jpn. J. Appl. Phys. 51, no. 9.(2012)

[3] H.Kawarada, *et al. Appl. Phys. Lett.***105**,013510 (2014).

[4] Y.Kitabayashi, H.Kawarada, et al. IEEE Electron Device Lett. **38**(2017)363.

[5]W.Fei, H.Kawarada et al., Appl. Phys. Lett.**116**,212103(2020)