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Vertical-type 2DHG Diamond MOSFET; Achieve High Current Operation of -3.4 A by Expanding Gate Width

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Abstract
In this paper, we report high current operation of vertical-type two-dimensional hole gas (2DHG) diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) with wide gate width (W_G). We fabricated devices with a W_G of 125 µm to 100 mm and evaluated the current characteristics. The maximum drain current of over -3 A was achieved with a W_G of 100 mm at V_{DS} = -50 V and V_{GS} = -20 V using pulse *I-V* measurement. This is the highest value for diamond FETs.

1. Introduction
Vertical power devices with low loss and high breakdown voltage are critical for realizing sustainable and energy-saving society. We have fabricated vertical-type diamond MOSFETs incorporating two-dimensional hole gas (2DHG) [1] and achieved high current density (~ 13 kA/cm^2) and low on-resistance (~ 3 mΩ·cm^2) [2]. Vertical-type diamond MOSFETs with a trench structure that can induce 2DHG disregarding the crystal orientation are promising candidates for next-generation p-channel power devices. Recently, p-channel power devices using gallium nitride (GaN) and silicon carbide (SiC) have been actively reported [3][4]. However, the performance of p-channel FETs in GaN or SiC is no more than 1-10 % of those of n-channel FETs. On the other hand, the performance of recent diamond p-FETs are comparable to those of GaN or SiC n-FETs [5]. Therefore, p-channel diamond power devices are expected to realize highly efficient complementary high voltage circuits such as inverters when combined with n-FETs such as GaN or SiC. In this work, we have fabricated vertical-type 2DHG diamond MOSFETs with trench structures whose gate width are 125 µm to 100 mm. As the result, the maximum drain current of over -3 A was obtained for 100 mm gate width at source-drain voltage (V_{DS}) of -20 V and a gate-source voltage (V_{GS}) of -20 V by pulse *I-V* measurement.

2. Device Fabrication
The cross-sectional view of the vertical-type 2DHG diamond MOSFETs is shown in Fig.1. First, the 500 nm undoped layer and 1 µm nitrogen-doped layer (nitrogen concentration: 1.0×10^{18} - 5.0×10^{18} cm^{-3}) were grown on the IIb (100) p+ diamond substrate (boron concentration: ~ 2×10^{20} cm^{-3}) by microwave plasma chemical vapor deposition (MPCVD). The trench was formed by inductive coupled plasma reactive ion etching with oxygen gas. After the trench formation, regrowth undoped layer (200 nm) was fabricated by MPCVD to induce the 2DHG. Source electrodes (Ti/Pt/Au) were formed, and hydrogen termination was conducted by remote plasma treatment. The 200 nm Al_2O_3 was deposited by high temperature atomic layer deposition method. Finally, the gate electrode was formed on the surface, and the drain electrode was formed on the back side of the substrate. The gate length, gate-drain length, trench length and trench width for each device were 2, 1.5, 3 and 60 um, respectively. In addition, these vertical-type devices had a gate overlapping structure [2], which minimized the device's active area and eliminated the source-gate length and gate-trench length. Fig.2 shows an optical micrograph of the device. The gate width per trench is 125 µm, and since there are 400 trenches in this device, the total W_G is 50 mm.

3. Results and Discussion
Fig.3 shows the I_{DS}-V_{DS} characteristics of a device with a W_G of 100 mm. The maximum drain current was -3.4 A with a W_G of 100 mm at V_{DS} = -20 V and V_{GS} = -20 V using pulse *I-V* measurement (duty ratio: 0.5 %). This drain current is the highest value in diamond FETs. This result indicates that a high drain current can be achieved in a multiple of trenches formed in one device by increasing the gate width. Fig.4 shows the I_{DS}-V_{GS} characteristics of 1 mm to 50 mm gate width at room temperature. On/off ratio was about 7 orders of magnitude for all dimensions at V_{DS} = -1 V. Furthermore, the threshold voltage (V_{th}) of these devices was approximately 30 V. From this result, it is shown that the nitrogen-doped layer functions as a current blocking layer and sufficient gate control is possible even when 400 trenches are formed in one device. Fig.5 shows the relationship between drain current ($|I_{DS}|$) and on-resistance (R_{ON}) as a function of W_G at V_{DS} = -20 V and V_{GS} = -20 V. The drain current tends not to be proportional to the gate width increase. When the W_G is less than 20 mm, the drain current increases at a rate of 0.133 A/mm, and above 20 mm, it increases at a rate of 0.018 A/mm. The on-resistance of 100 mm gate width device is 5.9 Ω. We consider that the dominant resistances exist on the p$^+$ diamond substrate and the source electrode, and that it could be eliminated by

improving the device structure. By improving this problem in the future, we think that the drain current can exceed -10 A operation.

4. Conclusion

We fabricated vertical-type 2DHG diamond MOSFETs with the gate width of 125 µm to 100 mm. The maximum drain current was -3.4 A with a W_G of 100 mm at V_{DS} = -20 V and V_{GS} = -20 V using pulse I-V measurement (duty ratio: 0.5 %). In the future, it is considered that the drain current will be increased by expanding the gate width and improving the device structure. Furthermore, these results showed that p-channel diamond MOSFETs have great potential to realize over -10 A operations and are excellent candidates for highly efficient complementary inverters.

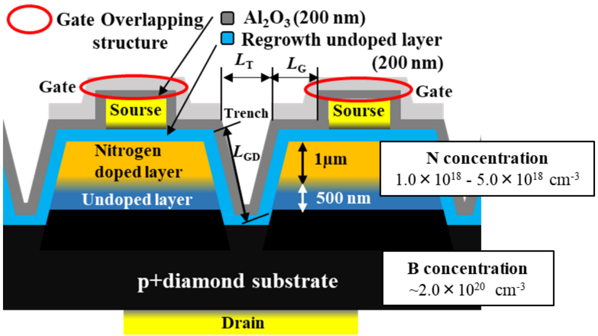
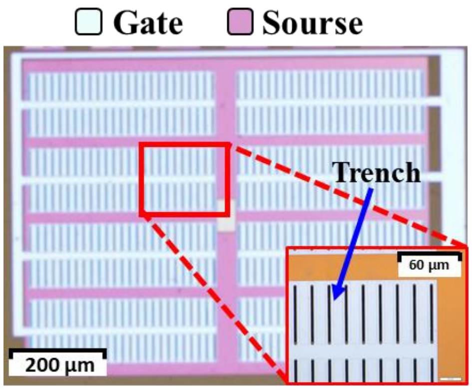


Fig.1 Cross sectional image of vertical-type diamond MOSFETs. L_{GD} is the drift region on the side wall of the trench. L_{SG} can be removed because it uses a gate overlapping structure.



400 Trenches (W_G: 50 mm)

Fig.2 An optical micrograph of the device (W_G of 50 mm). This device has 400 trenches. Trench length is 2 µm.

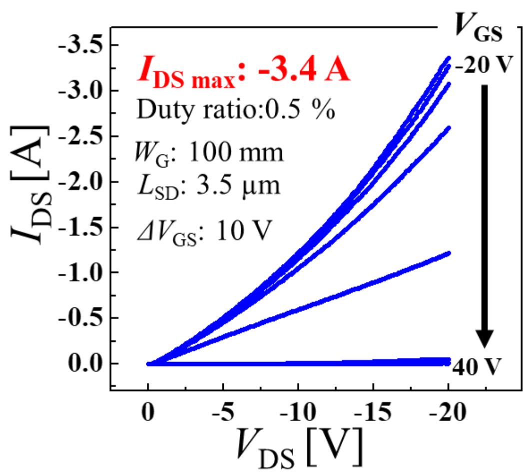


Fig.3 I_{DS}-V_{DS} characteristics using pulse *I-V* measurement. Duty ratio was 0.5 %. The maximum drain current was I_{DS} = -3.4 A at V_{DS} = -20 V and V_{GS} = -20 V. (W_G = 100 mm, L_{SD} = 3.5 µm, L_G =2 µm)

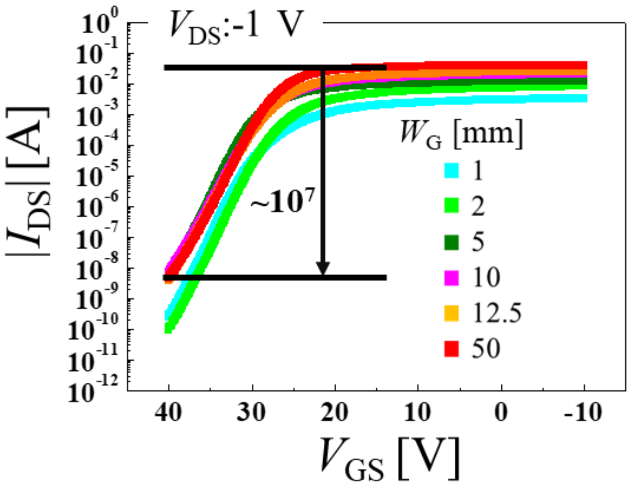


Fig.4 $|I_{DS}|$-V_{GS} characteristics of 1 mm to 50 mm gate width at V_{DS} = -1 V. On/off ratio is about 7 orders of magnitude for all dimensions. The threshold voltage (V_{th}) of these devices was approximately 30 V.

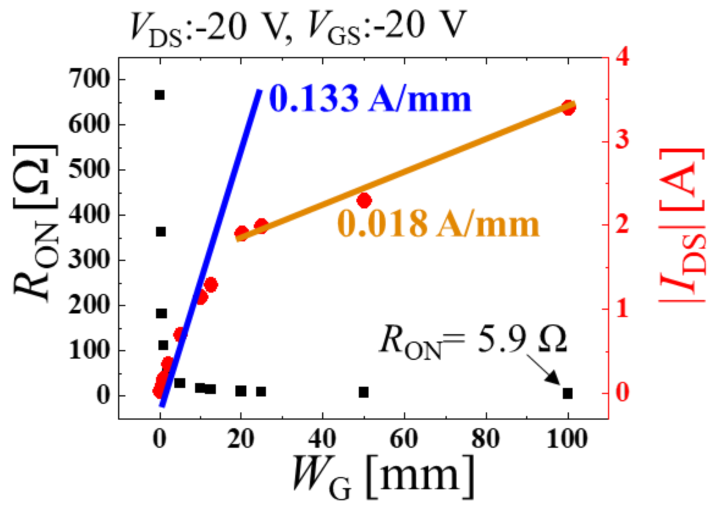


Fig.5 Relationship between drain current ($|I_{DS}|$) and on-resistance (R_{ON}) as a function of gate width (W_G) at V_{DS} = -20 V and V_{GS} = -20 V. R_{ON} is 5.9 Ω when the gate width is 100mm. The current increase amount of 0.133 A/mm is from 0.125 to 20 mm and that of 0.018 A/mm is from 20 to 100 mm. It was caused by source electrode resistance and substrate resistance.

Acknowledgements

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