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Novel Si stacking on β-Ga_2O_3 MOSFET structure enabling 0.59 mΩcm^2 of Ron,sp at 600V blocking voltage

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***Abstract*—Ga_2O_3 base vertical trench MOSFET achieving the normally-off operation is newly proposed, in which thin Si-MOSFET is stacking on n-type β-Ga_2O_3 drift layer. The state-of-the-art "Blocking layer" in p-Si is the key to relax the E-field in p-Si at Off-state and to obtain the current stability and the optimum Vth at On-state. Using this architecture, the normally-off operation with optimum Vth as 4V and an extremely low Ron,sp as 0.59 mΩcm^2 are estimated at 600V blocking voltage device.**

I. INTRODUCTION

Ga_2O_3 has emerged being thought as a promising material for the power switching devices among the wide band gap (WBG) semiconductor such as SiC or GaN from the cost and performance point of view. Even though Ga_2O_3 has many advantages over Si, it is hard to enable the normally-off type vertical trench transistor, because there exists no p-type Ga_2O_3.

Furthermore, MOS channel mobility of every WBG is very low due to its high surface state density, which rises Ron higher.

Due to the lack of p-type Ga_2O_3, FINFET structure [1] or another p-type material [2] has been proposed as the alternative to enable the normally-off operation for MOSFET. However, there has been currently no breakthrough to realize the vertical trench MOSFET that can achieve the high current density.

To overcome these drawbacks with maintaining the other advantages of Ga_2O_3, the novel MOSFET device architecture is proposed and verified by TCAD simulation.

II. DEVICE STRUCTURE

The proposed device is composed with Si-MOSFET stacking on 5um n-type β-Ga_2O_3 drift layer (Nd= 2e16cm^{-3}), as shown in Fig.1, where the direct bonding technology [3] can be utilized to form the p-n hetero-junction [4].

The direct bonding technology such as surface activated or fusion bonding enables the strong adhesion between different materials at RT with thermal stress free and an atomic level uniformity at the interface, that can maintain crystal periodicity as same quality as epitaxial growth. The Fig.2 shows the band diagram of Si (100)-Ga_2O_3 hetero-junction at the equilibrium condition. The trench gate penetrates the 1um thickness into p-Si bulk and another 1um depth to n-Ga_2O_3 drift region covering with 100nm gate Si-dioxide, where this film thickness will bring Qg*Ron FOM smaller. In order to protect the trench bottom from the E-field stress, Nitrogen ion implant is applied under the trench bottom, where the isolation layer is formed as the high resistive region [5]. Source (n^+) and bulk diffusion layer (p^+) are set on the p-Si surface, and the drain is set at the bottom of n-Ga_2O_3. In particular, the p-type "blocking layer" is partially (~0.3um) formed at the bottom of p-Si bulk with higher doping level (Na= 1e17cm^{-3}) than bulk to suppress the leakage between source and drain at "Off-state" and to regulate the channel current conduction at "On-state". The cell pitch of the proposed device is 2um where the mesa width is 1um.

III. DEVICE OPERATION AND SIMULATED RESULTS

Since it is so important to see what is brought by these kind of emerging technologies is, TCAD is the key to predict the characteristics and potential performance of newly proposed device structure. Here, AdvanceSoft's device simulation tool is used applying the physical property of β-Ga2O3 cited from the past works [6] [7].

In "On-state", it is so significant that the hetero junction is to be forced by the E-field from gate, thereby forcing the surface potential of n-Ga_2O_3, wherein Ec of Ga_2O_3 is 0.05eV higher than that of Si as in Fig. 2. It is also remarkable that the thickness of "blocking layer" is regarded as the "effective channel length" of MOSFET wherein the Vth and channel conductivity are determined by the thickness and the doping level of the p-type "blocking layer". Therefore, it will bring the less p-Si bulk thickness dependency on the channel conductance, which ensures the good bonding manufacturability in this proposed device. As a result, 0.59 mΩcm^2 of Ron,sp excluding the substrate resistance at Vg= 15V and 4.0V of threshold voltage at Vd= 1V are obtained using Yamaguchi mobility model [8] as shown in Fig.3 and Fig.4, respectively. This excellent performance is brought by the usage of fast channel mobility of Si-MOSFET in this prosed device.

Meanwhile, it is so important for "Off-state" to relax the electric field from Ga_2O_3 to Si less than 1/10. The solution is to narrowing the Mesa width in conjunction with the "blocking layer" explained above, these will prevent the electric field penetration into Si from the punch through or breakdown by the spatial effect and the doping control. Fig.5 shows the 2-D electric field distribution and potential in the whole device region simulated with Neumann condition for mirror boundary.

It is obvious that the averaged electric field within Si is small enough to bring the reciprocal of impact ionization factor α^{-1} [9] becomes 5um depth in Si. Fig.6 shows the comparison for wide/narrow mesa width and with/without blocking layer, respectively. The E-field at the gate bottom oxide is still large, which is around 5MV/cm, though the isolation layer can prevent the leakage current perfectly like an insulator. The E-field distribution can be relaxed by reducing the doping level or extending for the drift layer thickness, those have a trade-off relationship against on Ron. If the gate width is getting narrower, it is obvious that Ron,sp becomes smaller as the cell pitch shrinks less than 2um and below.

IV. SUMMARY

This proposed device structure will provide the fusion solution for Si- and WBG-MOSFET to achieve the high performance. To verify the new structures such as the bonding technology including hetero-junction, TCAD plays an important role to verify the device theory and determines the doping level and geometrical factors for the further trial chip production to optimize.

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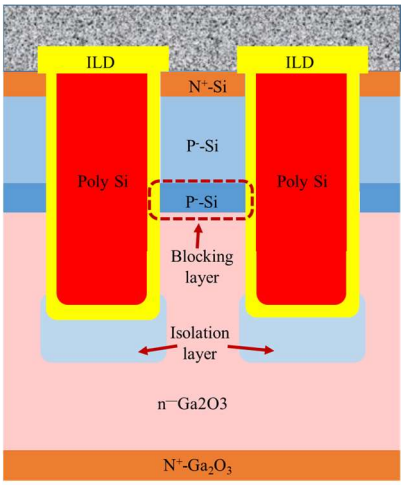


Fig.1 Cross section of the proposed device. SAB is applied to bond the Ga_2O_3 and Si at the interface with Ga_2O_3. .

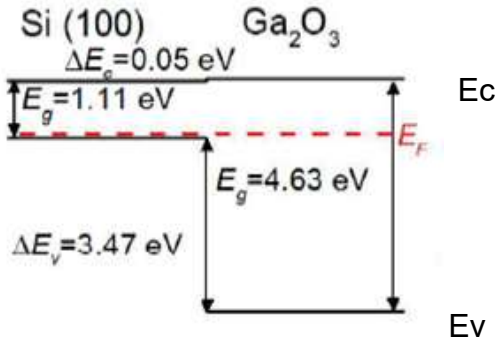
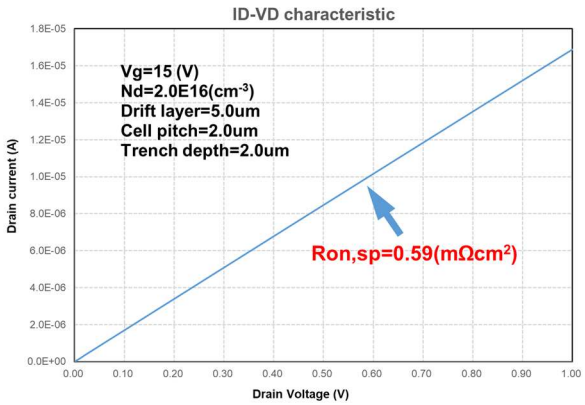


Fig.2 Band diagram of the proposed device illustrated at the equilibrium condition [6]. The electrons will get over the barrier height between Ga_2O_3 and Si by gate biasing.



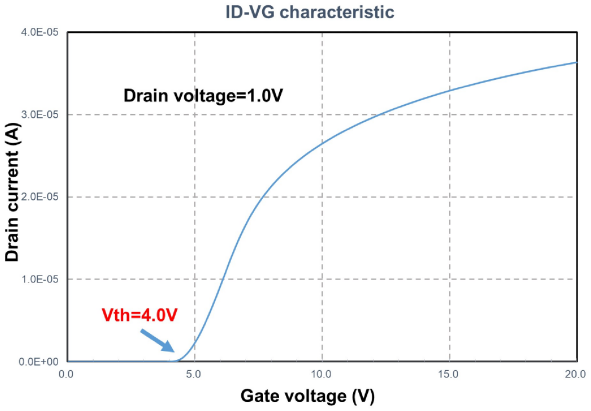


Fig.3 Id vs. V_d characteristic of the proposed device where 0.59mΩcm2 of Ron,sp is achieved at Von(Vd)= 1V.

Fig.4. Id vs Vg characteristic of the proposed device, where Normally-off operation is obviously achieved.

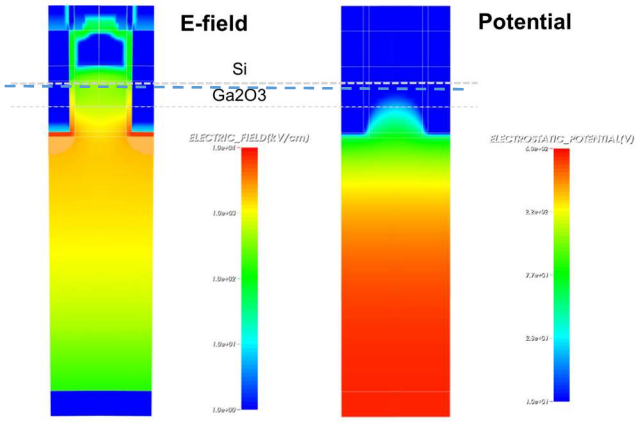


Fig.5 E-field and potential distribution at revered biasing with 600V on drain.

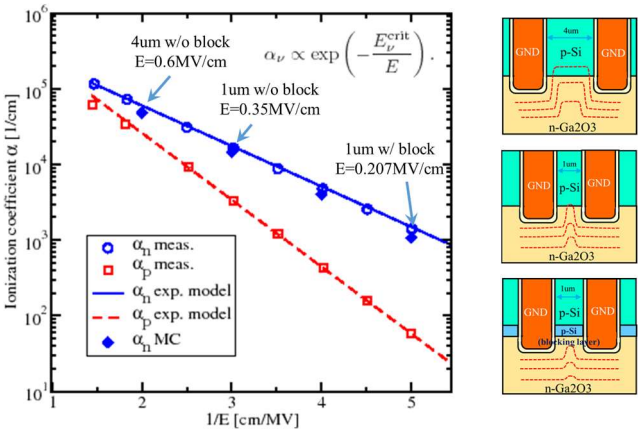


Fig.6. Impact ionization coefficient at the center of the proposed device. 1um channel width and block layer. α^{-1} will become 5um which is long enough to suppress the impact ionization in Si [9].