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Study of Leakage Mechanisms in III-V Nano-ridge diode on Silicon

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Abstract

An investigation of leakage mechanism in GaAs nano-ridge (NR) PIN diodes, based on the new technology of III-V on 300 mm Si, is reported. The impact of several mechanisms, such as SRH, TAT and BTB on the dark current is simulated using TCAD and compared with experimental data. As a result, the trap-assisted tunnelling is identified as dominant leakage mechanism. The tunneling process happens in the low-doped n-layer, and probably through the point defect in III-V material.

1. Introduction

In the last few decades, integration of III-V compound semiconductor on Si substrates has been identified as one of the promising routes to enable hybrid III-V/CMOS technology for different applications, such as logic and high frequency devices [1], light-emitting diodes [2], hybrid lasers [3], photodetectors [4] and solar cells [5]. The leakage current in such devices is an important performance parameter as it determines the signal-to-noise ratio, power dissipation, and reliability of the device. Various leakage mechanisms can dominate the dark current for III-V nano-ridge diodes, depending upon the shape, doping of nano-ridges, quality of epitaxial material as well as process related defect introduction.

In this work, we present theoretical and experimental investigation of various dark current mechanisms contributing to the leakage current of GaAs nano-ridge diodes on Silicon. Such nano-ridge devices are potential technology enablers in monolithic integration of III-V devices on Silicon.

2. Experimental details

The GaAs PIN diodes are grown by metal-organic vapour phase epitaxy (MOVPE) and illustrated in fig.1. Epitaxial growth is done on 300 mm Si (001) wafers (n = $1 \cdot 10^{18}\ cm^{-3}$) using nano-ridge engineering (NRE) approach [6-8]. In this way, defects, such as treading dislocations, are trapped in narrow trenches, which leads to an increased, defect-free, III-V volume used for devices fabrication. To reduce surface trap density, a 20-40 nm thick undoped InGaP layer is deposited in-situ after the growth of the GaAs diode layers. Details about the NR growth can be found in the Table I and previous publications [6-8]. After the NR growth, a thick SiO_2 planarization deposition step, which is formed by high-aspect-ratio process (HARP) atmospheric chemical vapour deposition (CVD), followed by the chemical mechanical polishing (CMP) process and metallization. The device length of the NR diodes is around 100 μm and width is 0.5-0.6 μm. The long length of nano-ridge is chosen to minimize the impact of faceted growth at the end of the edge of NR. To simulate electrical characteristics and understand the leakage mechanism, we used Sentaurus Device AC simulation tool. Electrical and defect characterisation are done using I-V, capacitance-voltage and Deep-Level Transient Spectroscopy (DLTS) techniques. To avoid additional electron-hole pair generation, electrical measurements are performed in the dark at room temperature.

Table I Structure of the fabricated GaAs PIN diodes.

Layer	Thickness, nm	Doping concentration, cm^{-3}
p^+	50	$9 \cdot 10^{18}$
p	150	$2 \cdot 10^{17}$
n^-	400	$3.5 \cdot 10^{16}$
n^+	200	$1 \cdot 10^{19}$

3. Results and Discussions

C-V measurements are used to verify the junction capacitance and the accurate doping profile of NR diode and calibrate it for Sentaurus Device simulations.

The total leakage current can be expressed as a sum of the bulk and surface components, $I_{tot} = I_{bulk} + I_{surf}$, where $I_{bulk} = I_{diff} + I_{Gen} + I_{Tun}$ at reverse bias. Depending on the bias voltage and temperature, diffusion (I_{diff}), generation-recombination (G-R) (I_{G-R}), trap-assisted tunnelling (TAT) and/or band-to-band tunnelling (BTBT) (I_{Tun}), components can be separated. The temperature dependent I-V analysis in reverse bias of the NR diodes, as shown in fig.2, is used to identify the source of leakage current. Diffusion or thermal current has a typical activation energy $E_{act} = E_g$ [9], SRH (Shockley-Read-Hall) generation-recombination shows $E_{act} = E_g/2$ [9], and $0.1\ eV < E_{act} < E_g/2$ for TAT [9-11]. The activation energy of the nano-ridge diodes is found to be in the range $0.2 - 0.48\ eV$, indicating the presence of the leakage mechanisms involving tunnelling.

DLTS results are used to define the defect distribution in the simulated nano-ridge structure. Typical DLTS spectrum for such nano-ridge diode is shown in fig.3, where narrow peak E1 around 350K corresponds to point defects and a broad H1 peak at 180K can be associated with the surface state density. Arrhenius plot shows the energy level of EL2 defects and surface states [12] in the lower inset. The bulk defects, which are detected in low-doped n-layer, and surface

state density are used for nano-ridge PIN diodes as fitting parameters. These parameters define bulk and surface component of the leakage.

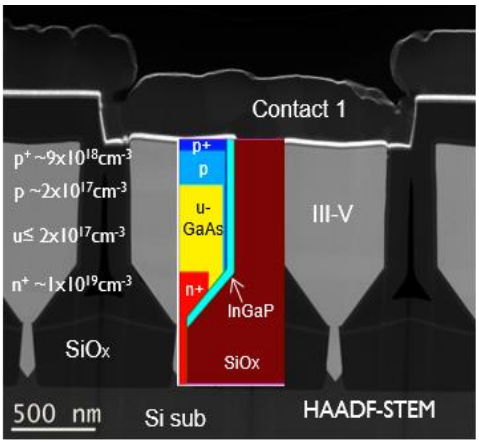

Fig. 1. Schematic and high-angle annular dark field scanning TEM (HAADF-STEM) image for GaAs Nano-ridge PIN diode.

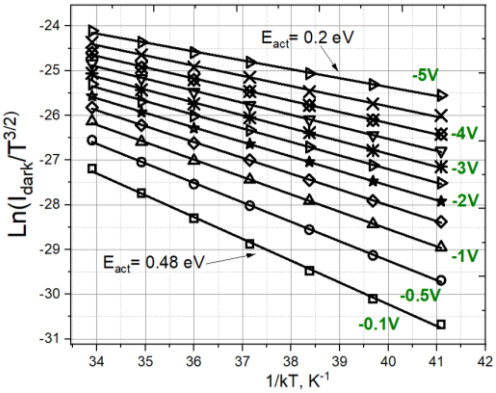

Fig. 2. Arrhenius plot for NR diodes at different reverse voltages.

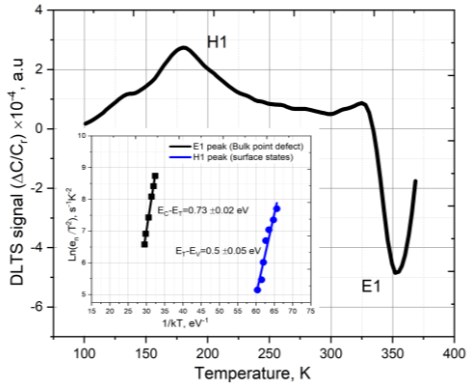

Fig. 3. DLTS spectrum for nano-ridge diode at V_R= -1V, t_w=100 ms, V_P =1.4V and t_P=1 ms; The lower inset shows Arrhenius plot corresponding to energy position of bulk defects and surface state density.

Based on the fitting with experimental data, we obtain the electrical characteristics using calibrated TCAD simulation models to construct the leakage current for NR PIN diodes shown in fig.4. Model A consists of a combination of diffusion and G-R (SRH) components, model B contains diffusion, generation-recombination and TAT components of the leakage. In case of model C, diffusion, G-R and BTB components are included as the leakage mechanisms. As shown in fig.4, simulated I-V matches well with experimental data in the forward region of the diode, except for high forward bias, where high series resistance is dominant for measured diodes. In the reverse bias region, model B seems to match better with measured data, while model A and C can only match in low field region (SRH dominant). This indicates that dominant leakage mechanism in nano-ridge PIN diodes is TAT component. Based on additional DLTS measurements, such trap-assisted tunneling process can happen through point defect, EL2 in the active layer of PIN diode.

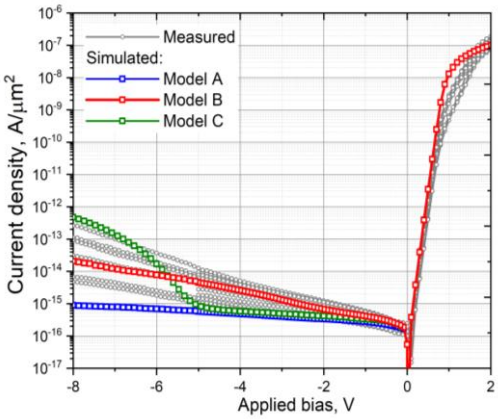

Fig. 4. Measured and simulated I-V characteristics of GaAs Nano-ridge PIN diode.

3. Conclusions

In this paper, we compared SRH, TAT and BTB models for GaAs Nano-ridge PIN diodes to identify the leakage current mechanism. It is shown that TAT current is dominant as the leakage current. The simulated electrical characteristics are in close agreement with the experimental data. It is shown through simulation and DLTS measurements that such trap-assisted tunneling process could be due to point defect, EL2, in the low-doped n-layer of the diode.

Acknowledgements

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References

[1] D. Nirmal and J. Ajayan. CRC Press, (2019).
[2] A. Aho et al., J. Appl. Phys., 115, (2019).
[3] Y. Han et al., Opt.7(2), (2020) 148-153.
[4] A. Farrell et al., Nano Lett., 17(4), (2017) 2420-2425.
[5] Y. Zhang and H. Liu. MDPI Crystals, 9(87), (2019).
[6] B. Kunert et al., ECS Trans., 75, (2016) 409-419.
[7] B. Kunert et al., Appl. Phys. Lett., 109, (2016).
[8] M. Baryshnikova et al., Cryst., 10(4), (2020).
[9] E. Simoen et al., *IEEE Elect. Dev. Lett.* 30, (2009) 562–564.
[10] C. Reynolds and A. Patel, J. Appl. Phys., 103, (2008).
[11] A. Czerwinski et al., J. Appl. Phys., 94, (2003) 1218.
[12] O. Syshchyk et al., Phys. Rev. Appl., (2020), submitted.