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High-Performance III-V-On-Si Transistor Technology Platform

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We demonstrate a III-V transistor technology platform that is fully integrated on silicon substrates by direct wafer bonding, and is fabricated with a Si CMOS-like process flow. Both DC and RF performance is analyzed, showing among the highest reported values for I_{ON} and f_t/f_{max} for integrated III-V FETs. In particular, we examine the effect of the channel heterostructure and source/drain spacers on device characteristics. These reports indicate the high promise of this type of technology for mixed-signal applications.

1. Introduction

III-V transistors have attracted significant research attention for their high carrier mobilities and unique features; they allow band structure engineering, direct band gaps and exhibit distinct physical phenomena [1]. For this type of transistor technology to achieve strong industrial impact, it must likely be embedded into standard CMOS technologies. This entails not only integration of III-V materials on Silicon substrates, but also the development of CMOS-compatible transistor process flows. In this work, we demonstrate IBM's III-V transistor technology and show key process modules that enable Si CMOS-compatible fabrication while maintaining strong device performance for both low-power and high-frequency applications.

2. Integration & Process Modules

Device fabrication is based on a Si CMOS-compatible replacement metal gate process flow, with epitaxially regrown self-aligned source and drain (S/D) contacts, similar to our previous reports [2], [3]. The channel comprises a 2 nm InP /10 nm $In_{0.75}Ga_{0.25}As$/20 nm InP quantum well, grown by MOCVD, directly integrated on buried oxide/silicon (NID) substrate by direct wafer bonding. Reference heterostructures with 20 nm InGaAs on BOX, as well as 10 nm InGaAs/20 nm InP on BOX were also fabricated. We also implement an RF-optimized device design with varying thickness of SiN_x S/D spacers (4 and 8 nm) and contact extensions underneath the spacers for reduced parasitic overlap capacitances and access resistances. Following integration of the channel by wafer bonding, an amorphous silicon dummy gate is deposited and patterened. SiN_x spacers are then formed in a self-aligned manner by atomic layer deposition and reactive ion etching. "Digital etching" – controlled oxidation and etching – is performed to create cavities under the spacers as well as remove the top InP layer in the channel regions. The cavities are then refilled in the MOCVD growth step with 25 nm highly doped InGaAs, forming the contact extensions underneath the spacers. Following, the dummy gate is stripped and the

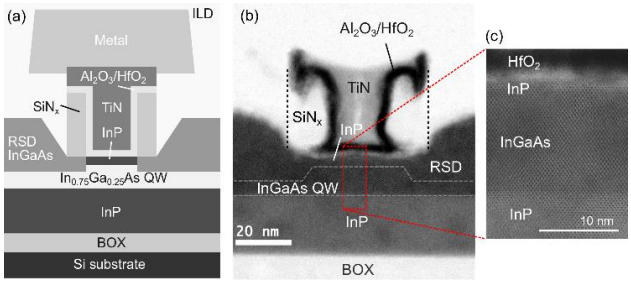

Fig. 1 (a) Schematic of the fabricated device. (b) Scanning TEM image of the cross-section of a fabricated device prior to W gate deposition. (c) High-resolution TEM image of the channel region.

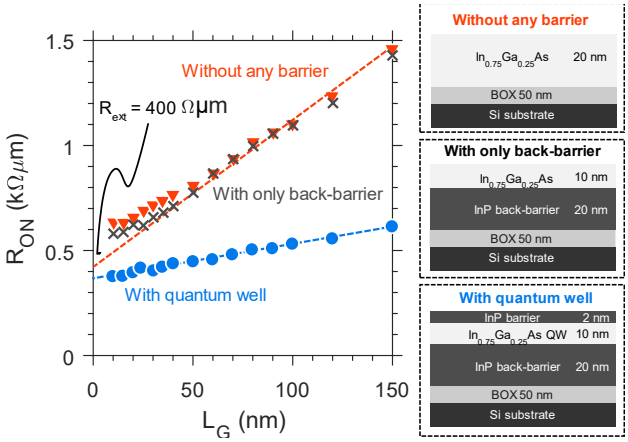

Fig. 2 On-resistance versus gate length is shown for three different channel heterostructures. As seen, the heterostructure with the thin InP top barrier is outperforming the other heterostructures. The slope of the curve is furthermore related to the channel carrier mobility, which is 3x higher for the heterostructure with the top-barrier, indicating that the reduced R_{ON} is due to reduced defect scattering at the oxide interface.

Al_2O_3/HfO_2 (EOT < 1 nm)/TiN gate stack is deposited by ALD. W gate metal is sputtered on the gate to further reduce gate resistance to enhance RF performance. Finally, M1 metal contacts are deposited and patterned, and the devices are annealed in forming gas. Fig. 1(a) shows a schematic of the fabricated device, while Fig. 1(b) shows a cross-sectional STEM image of a device prior to W deposition. Fig. 1(c) shows a high-resolution TEM image of the channel region. The layer thicknesses are determined from EDX scans along the channel.

3. Low-Power Logic Applications

Fig. 2 shows schematic figures for the three heterostructures studied in this work: Without any barrier, with only back barrier and with both top and front barrier. Detailed schematics

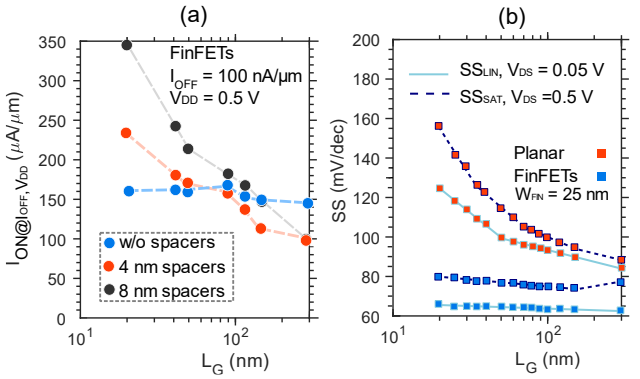

Fig. 3 (a) On-current, measured at fixed off-current of 100 nA/µm and bias swing of 0.5 V versus gate length, for different spacer thicknesses. The wider spacers are outperforming at scaled gate lengths likely due to a reduction of the parasitic bipolar effect, which causes an increase of the off-current. (b) Subthreshold swing versus gate length, comparing FinFETs and planar devices. The FinFETs exhibit a strong enhancement of scalability.

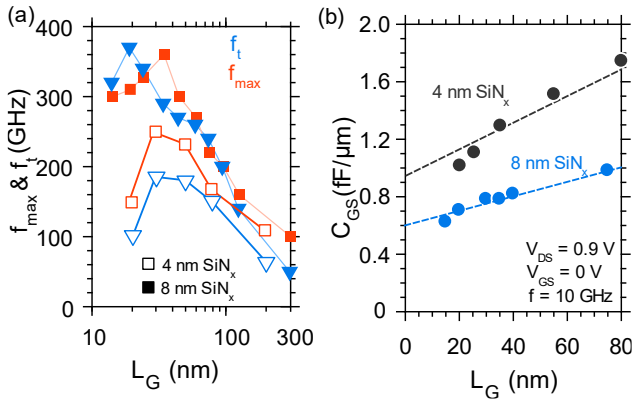

Fig. 4 (a) Cut-off and maximum oscillation frequency versus gate length. These values are determined from S-parameter measurements up to 45 GHz using a VNA. (b) Gate-to-source capacitance for the two different spacer thicknesses.

of the heterostructures are also shown. On-resistance, R_{ON}, versus gate length, L_G, is reported for the three heterostructures. An extrinsic resistance of 400 Ωµm is obtained from the y-axis intercept using linear extrapolation at long L_G. This value is comparable to that of state-of-the-art HEMTs. The extrinsic resistance is relatively independent of the channel type. Using TLM measurements, we determine the components of the extrinsic resistance: Ohmic contact resistance is 75 Ωµm, access resistance due to the 1 µm distance between metal and channel is 25 Ωµm, and the resistance due to the spacers is 100 Ωµm. The slope of the linear extrapolation is related to the channel carrier mobility, which can be calculated by approximating the gate capacitance. Using this method, electron mobility values of μ_e = 500 and 1500 cm^2/Vs are obtained for heterostructures without InP top-barrier and with a QW, respectively. This difference is attributed to reduced oxide interface traps and surface roughness scattering using the QW. Further increas of the top-barrier thickness can be expected to increase mobility, though it will also reduce the gate capacitance.

The on-current, defined at 0.5 V voltage swing from V_{GS} point where I_{OFF} = 100 nA/µm, is shown in Fig. 2(a) for three spacer thicknesses, 0 nm, 4 nm and 8 nm. Here are shown FinFET devices with fin widths of 25 nm and a heterostructure of 20 nm InGaAs on an InP back-barrier on BOX. As shown, the on-current is higher for wider spacers at scaled gate lengths. This can be attributed to a reduction of the parasitic bipolar effect, which is expected to be particularly severe in narrow-band gap channel materials prone to band-to-band tunneling. For long channel devices, this effect is weak and so the devices with no spacers outperform due to reduced parasitic resistances. Fig. 2(b) shows the subthreshold swing (SS) for both FinFETs and planar devices. FinFETs show significantly enhanced scaling properties and achieve steep slopes down to 20 nm gate lengths.

4. High-Frequency Applications

S-parameter measurements up to 45 GHz were performed to characterize the high-frequency properties of the fabricated devices. Off-chip two-port LRRM calibration as well as on chip open and short pad de-embedding up to M1 was performed. Here we examine the planar transistors with both top and bottom InP barriers. Devices comprise 2 gate fingers each 4 µm wide. Fig. 4(a) shows cut-off and maximum oscillation frequencies, f_t and f_{max}, versus gate length, for two spacer thicknesses. A maximum f_t of 370 GHz is obtained at L_G = 20 nm with 8 nm spacers. Clearly, thicker spacers are beneficial to RF performance at scaled gate lengths. This due to both reduced short-channel effects (which leads to reduced g_d and increased g_m at scaled L_G) and reduced parasitic source and drain capacitances. Fig. 4(b) shows the gate-to-source capacitance, C_{GS}, versus L_G for the two spacer thicknesses. Parasitic contributions to C_{GS} can be estimated by linear extrapolation to L_G = 0 nm. Accordingly, we obtain $C_{GS,par} \approx 0.6$ and 0.9 fF/µm, for 8 and 4 nm spacers, respectively. Since the overlap capacitance scales linearly with the thickness, these values show that the $C_{GS,par}$ = 0.6 fF/µm consists of 0.3 fF/µm overlap capacitance, and another 0.3 fF/µm coming from elsewhere in the device. This shows that performance can be further enhanced by parasitics reduction.

5. Conclusions

We have demonstrated a III-V transistor technology platform fully integrated on silicon substrates using direct wafer bonding, and fabricated using a Si CMOS-like process flow. Both DC and RF performance, I_{ON} and f_t/f_{max}, respectively, are among the highest reported for integrated III-V FETs, showing the great promise of this type of technology for mixed-signal applications.

Acknowledgements

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References

[1] H. Riel, et al., MRS Bull., 2014.
[2] C. Convertino, et al., IEDM 2019.
[3] C. Zota, et al., IEEE EDL **40**(4), 2019.