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Recent Progress of Silicon Carbide Super-Junction MOSFETs

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Abstract

A super-junction (SJ) device has been developed to improve the trade-off relationship between the breakdown voltage and specific on-resistance (R_{onA}). A multi-epitaxial growth method that consists of repetitions of an epitaxial growth and ion implantation had been used for fundamental demonstrations of SJ MOSFETs. Ion implantation along the crystal channel can be used to maximize the implantation depth as a promising technology in the future. A trench-filling epitaxial (TFE) growth method is expected for realizing wide voltage range SJ devices, because a thick SJ drift layer (> 20 μm) can be formed at one time. A 6.5 kV class SJ MOSFET was successfully fabricated that exceeds a 4H-SiC unipolar limit. Suppressing voids formed near the end of stripe-trenches is critical for a reduction of leakage current.

1. Introduction

A super-junction (SJ) device, in which alternating p- and n-type columns are located in a drift layer, is known to improve the trade-off relationship between breakdown voltage (V_{BD}) and on-resistance (R_{onA}). A Si-SJ device has been widely used, and the effect of the SJ structure in SiC has also been confirmed [1]. The key issue is the establishment of low-cost and stable fabrication process at this moment. Two major methods are commonly known to form the SJ structure: Multi-epitaxial (ME) and trench-filling epitaxial (TFE) growth methods. In the ME growth method, SJ structures are formed by repeating ion implantation and epi-growth while maintaining alignment of the implanted region in vertical direction. Therefore, making the dopant depth per one implantation as deep as possible is quite important. The first experimental demonstrations were conducted by using MeV-class ion implantation for deep implantation [1]. The TFE growth method is expected as a low-cost fabrication method for wide voltage range SJ devices. The method, however, requires a high aspect ratio trench formation, trench-filling epitaxial growth on off-angled SiC substrates, and accurate flattening process. Although these processes are more difficult than the ME growth method, the method is very attractive because a thick SJ structure can be realized in a single TFE growth step.

In this presentation, we discuss recent progress and critical issues of the ME and TFE growth method from the perspective of practical realization of SiC-SJ devices.

2. Experimental and Results

Multiple-epitaxial (ME) growth method

To confirm SJ effects on SiC material, we started to form two types of test elemental groups (TEGs) for evaluation of V_{BD} and the specific resistivity of the drift layer (R_{drift}) [1]. 4°-off (0001) 4H-SiC n-type substrates were used for TEG fabrications with the 1st n-type epi-layer, where the effective doping density was about 3×10^{16} cm^{-3}. A multiple random ion implantation (RII) of Al at the maximum ion energy of 8 MeV was used to form 3-μm-deep Al box profile. The pn-pillar width was 2.5 μm at equal intervals. Following the 1st RII, on all wafers except one, the 2nd epitaxial layer was grown on a partially implanted surface. Up to the 4th repetition of implantation and epi-growth was performed. As a result, the total SJ thickness became 11.9 μm by 4-times ME steps.

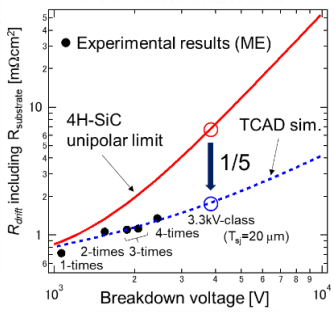

Figure 1 Tradeoff relationship between V_{BD} and R_{drift} of SiC SJ TEGs with TCAD simulation results and 4H-SiC unipolar limit.

As shown in Fig. 1, the experimental results on the R_{drift}-V_{BD} relationship for the 1st to 4th ME steps are well consistent with TCAD simulation results. The simulation result indicates 7-times ME steps is enough for 3.3 kV-class SJ devices where the SJ-depth estimated to 21 μm and the R_{drift} decreases to the one-fifth of 4H-SiC unipolar limit.

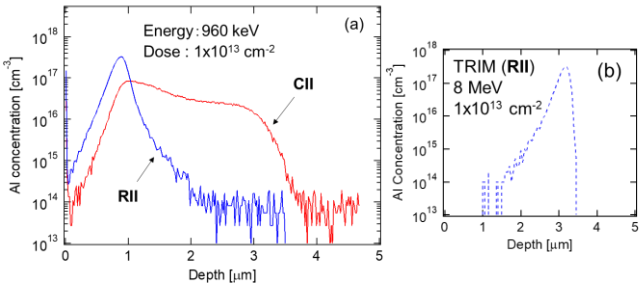

Figure 3 (a) SIMS profiles of Al channeled ion implantation (CII) and random ion implantation (RII). (b) TRIM simulation at 8 MeV.

As mentioned above, a high-energy RII at about 10 MeV is one of the candidates to reduce the number of ME steps. In addition to this, dozens of MeV implantation, which allows a depth of 7.5 μm at 26 MeV [2], should be considered as another candidate. Meanwhile, these high-energy RII requires a

special ion implanter different from conventional one with large lateral straggling depending on implantation energy. Alternatively, channeled ion implantation (CII) by using a parallel-scanning system is worth considering [3]. The maximum channeled range R_{max} of CII process is expected to be enhanced significantly with possibly a smaller lateral straggling. Fig. 2(a) shows Al depth profiles in case that CII of Al at 960 keV was performed toward [0001] channeling direction on 4°-off (0001) 4H-SiC n-type epitaxial wafer. The R_{max} increases from 1 to 3 μm by using CII, and the depth corresponds to that of RII at 8 MeV as shown in Fig. 2(b). The Al depth profile in Fig. 2(a) is characteristic of channeling implantation, which consists of a random component peak and a relatively flat channeling component. One must consider this profile and design the p-pillar Al distribution to control the charge balance.

Trench-filling epitaxial (TFE) growth method

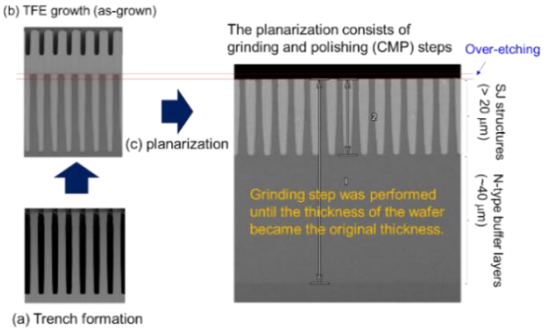

Figure 3 TFE growth method 4-step processes: n- (or p-) type initial epi-growth, (a) trench formation, (b) p- (or n-) type trench-filling epi-growth and (c) planarization.

The TFE growth method consists of 4-step processes, that is, the initial n-type epi growth, (a) trench formation, (b) p-type trench-filling epi-growth followed by (c) planarization. A partial SJ structure was used instead of a full SJ structure [4] for 6.5 kV-class SJ-MOSFET fabrication as shown in Fig.3. In the partial SJ structure, an n-type buffer layer is connected to the bottom of the SJ structure. For suppressing the tilt of the film grown on the mesa top during TFE growth, the stripe-trenches were formed along the [11-20] direction with an accuracy less than 0.5 ° at least [5].

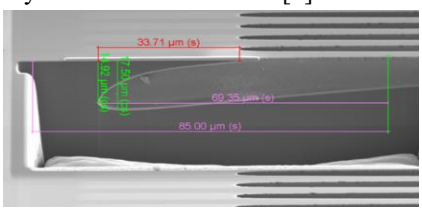

Figure 4 Unintentional voids, which cause the leakage current, formed near trench edges during TFE growth.

Large leakage current was observed at a pn junction in the partial SJ structure [6]. Emission analysis revealed that the cause of leakage current was unintended voids formed near the trench edges during TFE growth. Fig. 4 shows the cross-sectional FIB-SEM image of the void region. This result suggests an existence of leakage path on the edge region of each stripe-trench, although the formation mechanism and detailed structure of these voids are not clear yet [7]. We confirmed the leakage current of pn junction TEG was drastically decreased by separating these voids by cleavage [6] and by tapered trench with nitrogen implantation [8].

6.5 kV-class SJ-MOSFET fabrication

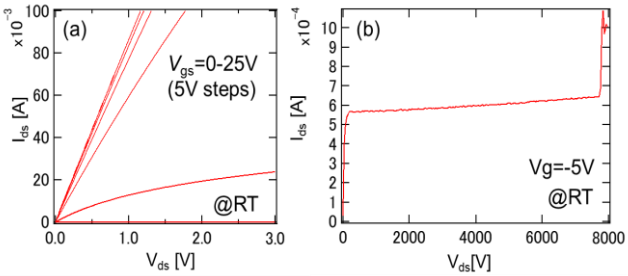

Figure 5 Forward and blocking characteristics of 6.5 kV-class SJ-MOSFETs formed by TFE growth method without separating voids.

6.5 kV-class SJ MOSFETs were fabricated on the partial SJ wafer, where the Al concentration in the SJ region and in the buffer layer was, respectively, designed to be 1.5×10^{16} and 2.0×10^{15} cm^{-3}. A cell pitch of SJ MOSFETs was 10 μm, corresponding to twice the pn column pitch. Figs. 5(a) and 5(b) show forward and blocking characteristics, respectively. The R_{onA} and V_{BD} measured at RT were 17.8 mΩcm^2 and 7.8 kV, respectively. The large leak current is caused by the void at the end of stripe-trenches described above. Temperature dependence of R_{onA} of another device fabricated on the same wafer revealed that the R_{onA} was 18.2 mΩ·cm^2 at RT and 48.7 mΩ·cm^2 at 175°C. The R_{onA} values are half of the state-of-the-art 6.5 kV-class SiC MOSFET with an n-type drift layer [6].

3. Summary

Strong potential of SiC SJ MOSFETs has been demonstrated experimentally using both ME and TFE growth methods. This demonstration shows that SJ devices will upgrade SiC unipolar power devices. Critical issues are to establish a highly-productive and low-cost manufacturing method of the SJ structure with high production yield.

Acknowledgements

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