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Anisotropic temperature distribution causing an incremental trend in the saturated drain-current of SiC MOSFET

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Abstract

Generally, drain current (I_d) of transistors saturates at a high drain voltage. However, SiC metal-oxide-semiconductor transistors show an incremental trend in its saturated-I_d behavior. Device simulation reveals that anisotropic temperature distribution causes this unusual characteristic. This temperature inhomogeneity occurs during off-to-on transient switching, which generates a higher temperature in the channel region than that in the other areas of a SiC die. Thus, it enhances electron mobility by decreasing the Coulomb scattering owing to its positive temperature coefficient.

1. Introduction

The SiC metal-oxide-semiconductor field-effect transistor (MOS) is a promising device for high power applications because of its high switching speed [1]. The switching repeatedly operates between high drain-voltage (V_d) with low drain-current (I_d) and low-V_d with high-I_d. Consequently, the I_d as a function of V_d and gate-voltage (V_g) in a high-V_d and high-I_d (HVHC) range determines circuit operations for power supply [2].

We have previously developed a methodology to measure the I_d–V_d characteristic in the HVHC range (HVHC I_dV_d) [2, 3]. The HVHC I_dV_d measurements demonstrate an incremental trend in the saturation region of I_d (I_{dsat}). Short channel effect (SCE) and/or drain-induced barrier lowing (DIBL) causes this unusual I_{dsat} behavior [4], but only very lower-I_d and -V_d areas were analyzed than those generally used in the power supplies that employ the SiC MOSs. Accordingly, this study aims to investigate the incremental I_{dsat} occurrence in the HVHC I_dV_d.

In this study, we employed device simulation with the measured HVHC I_dV_d data of a SiC MOS. First, the HVHC I_dV_d data were measured at 298 K and were used to specify the parameters in the simulation. The switching operations were virtually reproduced in the simulation. This causes a high temperature locally in the channel region that enhances electron mobility through reduced Coulomb scattering. This scattering factor is predominant in the SiC MOSs [5]. Our simulation that includes this mechanism reproduces the incremental I_{dsat} of the SiC MOSs.

2. Experimental and Simulation

We use the measurement method reported in [3] to obtain the HVHC I_dV_d of a SiC MOS (SCT2080KE, ROHM). A two-dimensional device simulation (TCAD), Sentaurus Device from Synopsys, was used to create the HCHV I_dV_d of the SiC MOS.

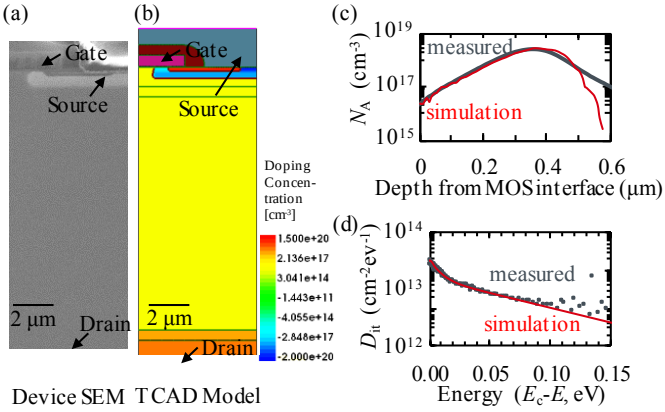

Fig.1 (a) SEM cross-section (b) TCAD modeled half unit-cell structure of the SiC MOS (c) N_A profile (b) D_{it} profile.

Figs. 1(a) and (b) show the scanning electron microscopy (SEM) images of the cross section of the half-cell structure of a SiC MOS and corresponding drawing for simulation, respectively. Fig. 1(c) shows the secondary ion mass spectroscopy (SIMS) profile of acceptor doping concentration (N_A) at channel region and N_A set in simulation to match the SIMS profile in the range of 0–0.5 μm. Generally, acceptor- and donor-like interface traps exist at the MOS interface [6]. We incorporated an acceptor-type interface trap density (D_{it}) and positive fixed charge as a donor-type interface trap density (D_{fc}) at the interface. The D_{it} is set to include the Coulomb scattering for channel mobility as given below.

$$(1)\quad \mu_C = \frac{\mu_1 \left(\frac{T}{300\ \mathrm{K}}\right)\left\{1+\left[c/\left(c_{\mathrm{trans}}\left(\frac{N_c}{N_0}\right)^{\eta 1}\right)\right]^{\upsilon}\right\}}{\left(\frac{N_c}{N_0}\right)^{\eta 2} D(x) f(E_\perp)} \qquad [7]$$

where, the notations are the same ones shown in [7].

Fig. 1(d) shows the D_{it} in simulation and D_{it} that were measured using the method reported in [8]. We adjusted the $D_{fc} = +1.5 \times 10^{12}$ cm^{-2} for the simulated I_dV_d to coincide with the measured I_dV_d at $V_g = 9$ and 11 V.

We utilized the values of the thermal conductivity and heat capacitance of the materials used in the device provided in [9]. We assumed that heat does not dissipate from the gate and source but dissipates from the drain at 298 K or 425 K. The drain contact is factored in as thermal resistance. The

thickness of the SiC substrate is 200 µm.

The self-heating energy, P, is estimated as reported in [3]. P is used to simulate the temperature distribution in the unit-cell MOS structure. The simulated temperature affects the electron channel mobility as shown in Eq.(1), thus leading to the simulated HVHC I_dV_d to include the effects of temperature distribution.

3. Result and Discussion

Figs. 2(a) and (b) show the measured and simulated HVHC I_dV_d at 298 K and 425 K, respectively. Here, the simulations ignore P.

All the simulated I_d curves exhibit saturation, i.e., this model does not demonstrate the incremental I_{dsat} behavior. I_{dsat} is greater at 425 K than at 298 K. This suggests that the device temperature would cause the incremental characteristic.

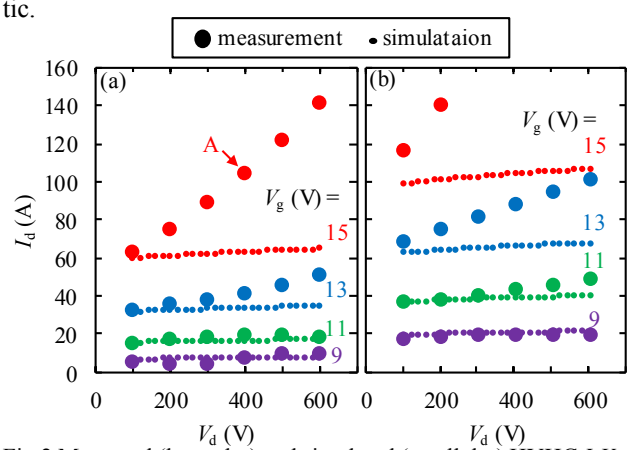

Fig.2 Measured (large dot) and simulated (small dot) HVHC I_dV_d (a) at 298 K (b) at 425 K.

Thus, further simulations incorporated P. First, we simulated the temperature distribution in the structure at point A, as shown in Fig.2(a), where I_d =105 A, V_d = 400 V, and V_g = 15 V. The results are summarized in Figs. 3(a), (b), and (c).

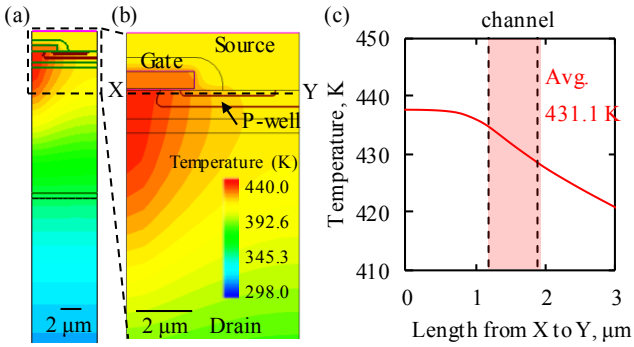

Fig.3 Temperature distribution at the operation point A in Fig.2(a). The contour plots of temperature of (a) the large area and (b) the area near the channel. (c) The temperature distribution along the X–Y plane defined in (b)

Figs. 3(a) and (b) show that the heat generation centers near the channel region, and the temperature is increased significantly from 298 K even under 298 K-ambient temperature measurement. The pale pink zone in Fig. 3(c) corresponds to the channel and its average temperature reaches 431.1 K. As this temperature approximates to 425 K, the simulated I_d = 104.6 A at 425 K, as shown in Fig.2(b), for V_d = 400 V and V_g = 15 V also approximates to the measured I_d at 298 K. This strongly indicates that the non-uniform temperature distribution causes the unsaturated I_{dsat}. The Coulomb scattering caused by the MOS interface defects dominates the channel mobility of the SiC MOS [5]. Further, high temperature reduces the Coulomb scattering to enhance the channel mobility [7]. A high temperature near the channel decreases the Coulomb scattering to enhance the channel electrical conductivity, which leads to a higher I_{dsat} than that expected according to simple theory.

Figs. 4(a) and (b) show the simulation results at 298 K and 425 K, respectively, where P is factored in for the SiC MOS HVHC I_dV_d. As previously mentioned, the simulated results are in correspond well with the measurement curves. Thus, the anisotropic temperature distribution near the channel region can explain the cause of the incremental trend in the I_{dsat} that is generally observed in the HVHC I_dV_d of SiC MOSs.

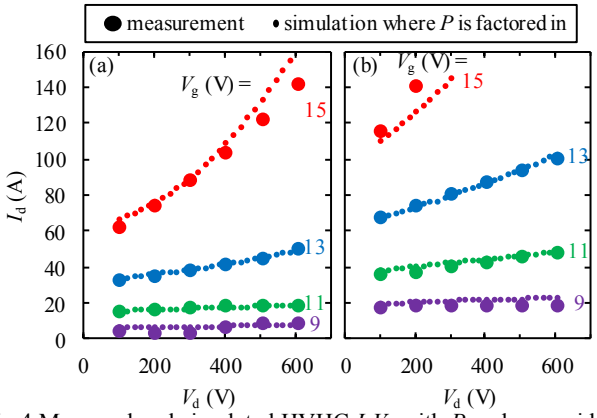

Fig.4 Measured and simulated HVHC I_dV_d with P under consideration at (a)298 K, and (b) 425 K.

3. Conclusions

Our simulation studies show that the general phenomenon of increasing I_{dsat} of the SiC MOSs in HVHC I_dV_d is highly possibly caused by the anisotropic temperature distribution owing to the positive temperature dependence of the Coulomb scattering.

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