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Influence of Interface Traps on the Shape of Split *C-V* Curves of 4H-SiC MOSFETs at Inversion

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Abstract

The shape of C_{GC}-V curves obtained by the split C-V technique was investigated for n-channel 4H-SiC MOSFETs. The ledge shape appeared at inversion, and it can be explained by taking interface traps into consideration. Comparison between the simulated C_{GC}-V curve without interface traps and the measured curve revealed that the capacitance of interface traps was in series with the oxide capacitance.

1. Introduction

SiC is one of the most promising wide-bandgap semiconductor for power devices [1]. However, the high density of interface states (D_{it}) in 4H-SiC/SiO_2 structures leads to the poor properties of 4H-SiC MOSFETs [2]. N-type SiC MOS capacitors are usually utilized to estimate n-channel SiC MOSFET performance, because D_{it} measurement using the MOS structure is only possible on the majority carrier side due to the wide bandgap of SiC. However, the differences in the dopant elements of *n*-type and *p*-type substrates may affect the SiO_2/SiC interface properties, so the D_{it} near E_C should be evaluated from measurement performed on n-channel 4H-SiC MOSFETs with *p*-type layer. In this work, the split *C-V* technique was applied on n-channel 4H-SiC MOSFETs to investigate interface traps in 4H-SiC/SiO_2 structures, though this technique is usually adapted to mobility evaluation [3]. By applying the split *C-V* technique on n-channel 4H-SiC MOSFETs, a ledge was found on the C_{GC}-V curve. The similar C_{GC}-V curves were reported before [4, 5], but the origin of the ledge was not explained clearly. Here, we focus on the ledge shape and found that the ledge is caused by interface traps.

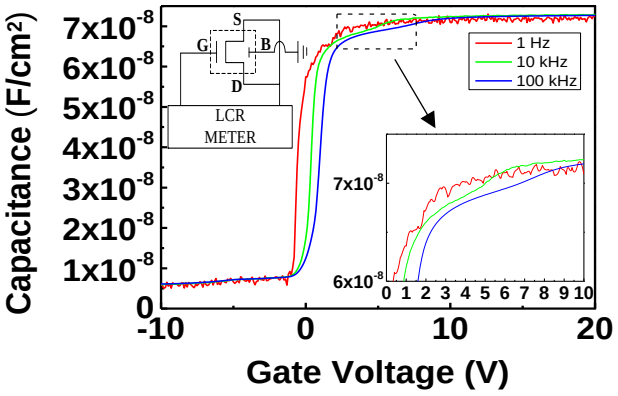

Fig. 1. C_{GC}-V curve of 4H-SiC MOSFET.

2. Experiments

Split *C-V* measurements were performed at various frequencies on n-channel 4H-SiC MOSFETs with a gate voltage range between -10 V and 20 V. The gate oxides (t_{ox} = 50 nm) of the sample were formed by dry oxidation followed by nitridation at 1250°C for 10 minutes. The equivalent measurement circuit is shown as the inset (left side) in Fig. 1 [6].

3. Results and Discussion

Figure 1 shows C_{GC}-V curves with different frequencies. In Fig. 1, there is a ledge (enlarged view of the ledge is shown as the inset in Fig.1) as gate voltage is about 3.5 V, which is above the threshold voltage of the MOSFET. Figure 1 also indicates that the ledge shape is frequency dependent. It can be seen that the ledge disappeared when measured at 1 Hz. This can be explained as when the frequency of the AC gate voltage is too low like 1 Hz, all interface traps immediately change occupancy in response to the AC gate voltage. Therefore, the C_{GC}-V curve becomes smooth. As frequency increases to a large value, interface trap response decreases to the AC gate voltage. So the ledge shape measured at 100 kHz becomes less steep than that measured at 10 kHz. The frequency dependency of the ledge shape implies the ledge is caused by interface traps near E_C [7].

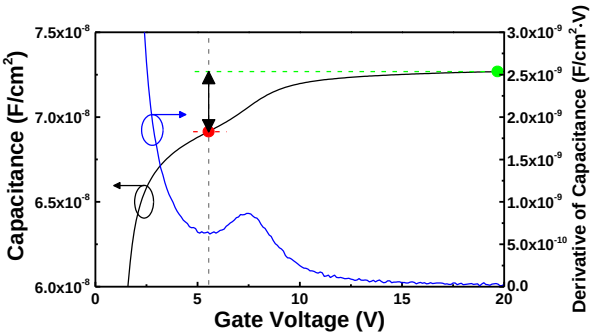

Figure 2 shows the split *C-V* curve and its derivative measured at 100 kHz. Point A on the C_{GC}-V curve is defined as the corresponding voltage when the differential curve (blue line) reaches a local minimum because this point is the slope turning point of C_{GC}-V curve. The height of ledge is indicated by the arrow in Fig. 2. The height of the ledge is defined as the height from point A (red dot) to point B (green dot, the maximum capacitance point). The height of ledge

reflects the capacitance caused by interface traps.

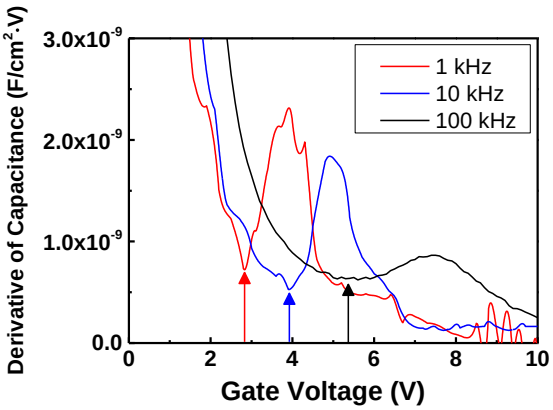

Fig. 3 Frequency dependence of derivative of capacitance.

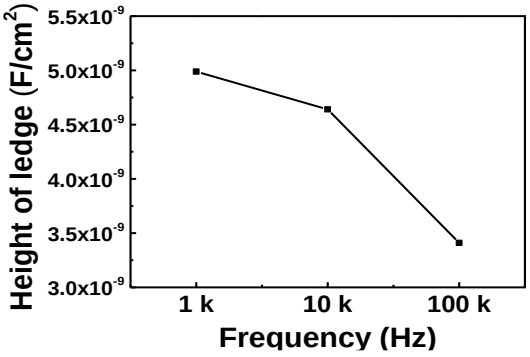

Fig. 4 Relationship between height of ledge and frequency.

Figure 3 shows the relationship between the derivative of capacitance and frequency. The local minimum point shifted to a higher gate voltage when the frequency increased. With increasing frequency, the traps which can follow the AC gate voltage should be closer to the conduction band so that the traps can exchange electrons with conduction band [8, 9]. The relationship between the height of the ledge and frequency is shown in Fig. 4. As shown in Fig. 4, the

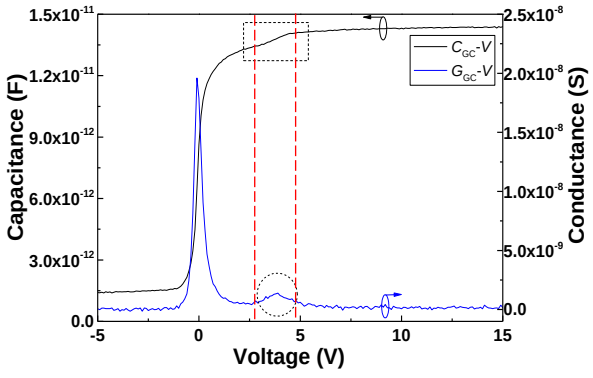

Fig. 5. C_{GC}-V and G-V curve at 1 kHz

height of the ledge decreases with increasing frequency because interface traps cannot immediately response to the AC gate voltage [10].

Figure 5 shows the C_{GC}-V and G_{GC}-V curves at 1 kHz. The peak, which is circled on the G_{GC}-V curve in Fig. 5, appears at the same voltage (about 3.5 V) when the ledge appears on the C_{GC}-V curve. This peak on the G_{GC}-V curve implies that there is an energy loss caused by interface traps near E_C. At DC gate voltages lower than 3 V or higher than 4 V, interface traps do not respond with the AC gate voltage, thus the energy loss decreases.

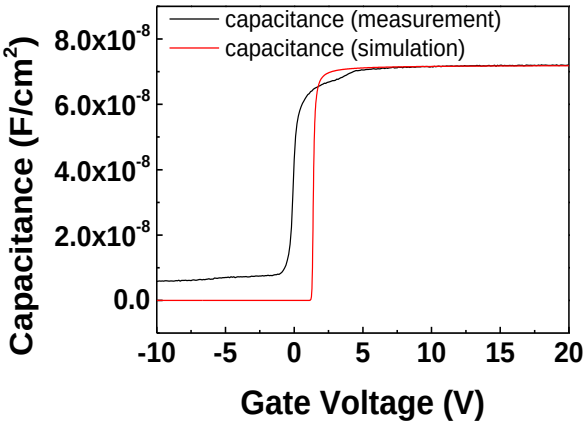

Fig. 6. Simulated and measured C_{GC}-V curve

The simulated C_{GC}-V curve without influence of interface traps is shown in Fig. 6 together with the measured C_{GC}-V curve. The simulated capacitance is higher than the measured curve where the ledge occurs. Therefore, the capacitance caused by the interface trap is considered in series connection with the oxide capacitance.

4. Conclusion

Split C-V technique was applied on n-channel 4H-SiC MOSFETs, and a ledge was found on the C_{GC}-V curve. By defining the slope turning point of the ledge, we found that the height of ledge showed frequency dependency. We explained the cause of the ledge shape of the C_{GC}-V curves to be interface traps.

Acknowledgement

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