Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp245-246

Effect of thick nitride layer on the RF performance in GaN HEMTs on 3C-SiC/Si

Arijit Bose[1], Debaleen Biswas[1], Shigeomi Hishiki[2], Sumito Ouchi[2], Koichi Kitahara[2], Keisuke Kawamura[2] and Akio Wakejima[1]

[1] Department of Electrical and Mechanical Engineering
Nagoya Inst. of Tech., Nagoya 466-8555, Japan
Phone: +81-70-3968-0541 E-mail: arijeetbosu@gmail.com
[2] SIC Division, Air Water Inc.,
Azumino, Nagano 399-8204, Japan
Phone: +81-263-71-2510

Abstract

We studied the RF performance of GaN HEMTs on 6-inch Czochralski (Cz)-Si substrate by introducing a thick (8.0 µm) nitride layer via a 3C-SiC intermediate layer. The obtained f_T and f_{max} of 2-µm gate-length devices were 4.4 and 11.5 GHz respectively. The Hall measurements showed excellent mobility of ~2000 cm^2/V-s and sheet resistance of ~400 Ω/sq. The maximum drain current density of 490 mA/mm and maximum transconductance of 129 mS/mm were obtained from the static and transfer characteristics. The S-parameters of open pad structures showed outstanding temperature stability up to 125 ºC. Load-pull measurements of the device exhibited 2 GHz continuous wave power density of 3.4 W/mm and maximum power added efficiency of 49.5% along with 17.6 dB gain.

1. Introduction

GaN HEMT stands as an excellent potent candidate for the high-power and high-frequency applications because of its unique combination of abilities like high-breakdown field and high electron saturation velocity [1]. Despite of having certain advantages, the high-production cost of SiC and GaN substrates hinders the wide application of GaN based devices. In this context, GaN-on-Si based devices enable both state-of-the-art high-frequency, high-power performance and cost-effectiveness. The critical challenge of large lattice and thermal co-efficient mismatch between GaN and Si was suppressed by introducing a SiC intermediate layer which also helped to grow a thick high-quality nitride layer on Si [2].

In this work, we introduced a thick nitride layer on Cz-Si substrate to eliminate the effect of low resistivity of Si and significantly reduce the parasitic pad capacitance to get an improved frequency performance. Moreover, we measured temperature dependency to see the device performance for high-power applications. The device showed an excellent competitiveness by achieving 4.4 GHz cutoff frequency for 2 µm gate-length device and unaltered pad characteristics during temperature dependent S-parameter measurements. The load-pull analysis exhibited PAE of 49.5% at V_d = +20 V with 17.6 dB gain under class A biasing operation.

2. Growth and fabrication

The 8 µm thick nitride layer was grown by metal oxide chemical vapour deposition (MOCVD) on the commercially prepared 1 µm 3C-SiC(111)/Cz-Si substrate with a diameter of 6-inch. The Cz-Si crystal have higher elastic limit than a Float Zone crystal and the SORI of the 6" substrate after nitride deposition was stably controlled less than 50 µm. The crack free nitride epilayer was achieved with edge exclusion of 5 mm. A schematic cross section of the device is shown in Fig. 1.

For the device fabrication, firstly BCl_3 plasma-based mesa isolation etching was performed followed by the source and drain area patterning by UV photolithography. The ohmic contacts were made by rapid thermal annealing of the de-posited Ti/Al/Ni/Au metal stack, at 850 ºC for 30 seconds in the N_2 environment. Finally, Ni/Au metal stack was deposited for the gate electrodes.

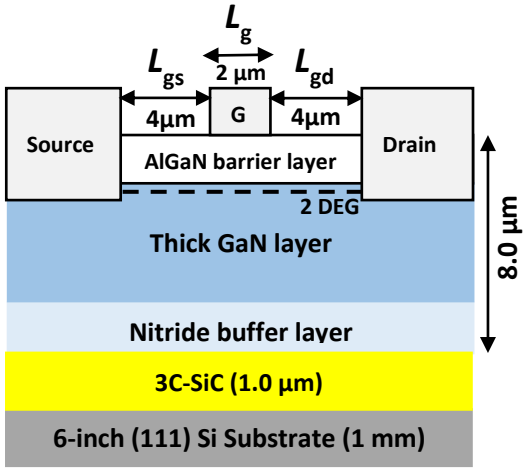

Fig. 1 Schematic cross-section of the fabricated AlGaN/GaN HEMT.

3. Results and discussions

The DC measurements exhibited maximum drain current density ($I_{d,max}$) of 490 mA/mm at V_g = +2 V and maximum trans-conductance ($g_{m,\,max}$) of 129 mS/mm at V_g = -1 V. We achieved the 2DEG mobility (μ) of approximately 2000 cm^2/V-s and carrier concentration (N_S) of 7×10^{12}/cm^2 from the room temperature Hall measurements.

The cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were extracted from the small-signal current

gain (|*H*21|) and the extrapolated unilateral power gain (*U*) respectively. Fig. 2 represents the maximum f_T of 4.4 GHz and f_{max} of 11.5 GHz at peak g_m biasing for the device with gate-length of 2 µm. This value of f_T is perfectly on the state-of-art with the previous reports of GaN HEMTs on Si and SiC substrates.

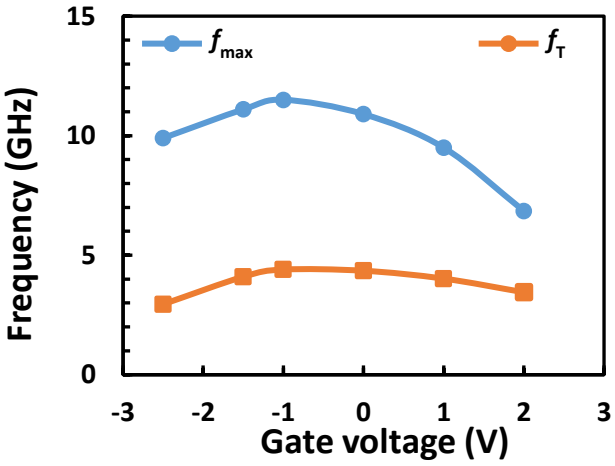

Fig. 2 The gate bias (V_g) dependency of f_T and f_{max} for the 2-µm gate-length device.

The on-wafer S-parameter measurements were performed on the open pad structures to extract the value of parasitic pad capacitances. The obtained pad capacitance of gate (C_{pg}) and drain (C_{pd}) side were 0.054 and 0.063 pF, respectively. Fig. 3 represents the excellent temperature stability of pad characteristics up to 125 ºC, which is greatly advantageous to prevent the low efficiency at large back-off region of power devices. Moreover, there is a chance of charge carrier generation at high temperatures which increase the pad capacitances and that lead to degraded frequency performance. In our case, it is very evident that no carrier generation occurred up to 125 ºC in the thick nitride layer or the SiC intermediate layer.

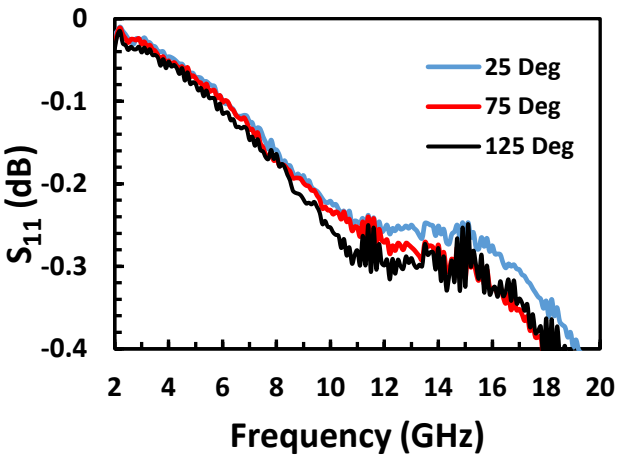

Fig. 3 Temperature dependent (25–125 °C) S-parameter (S_{11}) of open pad structure in the frequency range (2-20 GHz).

A small-signal equivalent circuit was applied to extract the intrinsic and extrinsic parameters and the extracted data perfectly validated our experimental result. The introduction of thick nitride layer has verified our assumptions of having very low parasitic capacitance by curbing the RF leakage through it. The temperature stability has also established the device to be useful for high-power applications.

The load-pull measurement exhibited 49.5 % PAE while delivering 3.4 W/mm output power with a saturated power gain of 17.6 dB at 2 GHz fundamental frequency (Fig. 4). The transistor was biased for class A operation where V_d was +20 V and V_g = -1.5 V.

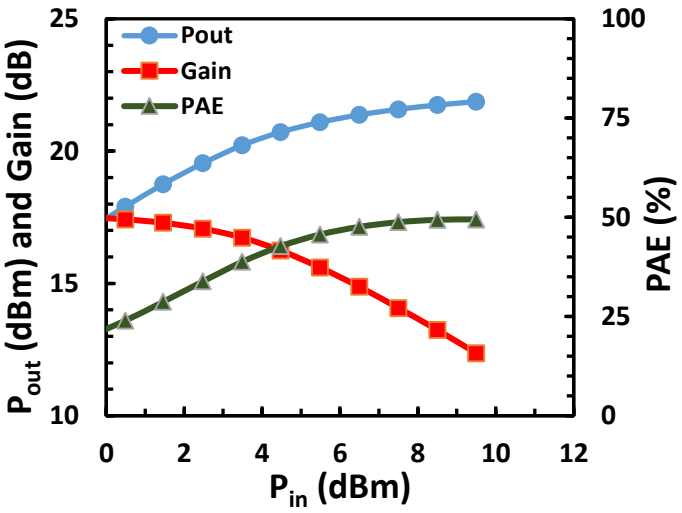

Fig. 4 The CW power measurement of 2-µm gate length AlGaN/GaN HEMT at 2 GHz fundamental frequency, where V_d = +20 V and V_g = -1.5 V.

3. Conclusions

In summary, the enhanced RF performance of the fabricated GaN HEMTs was achieved due to the introduction of 8.0 µm thick nitride layer, grown via 3C-SiC intermediate layer. It significantly suppressed the low resistivity effect of Si and reduced the pad capacitances. The comparable f_T of 4.4 GHz for 2 µm gate-length device, temperature stability of pad measurements and output power density of 3.4 W/mm clearly establish the presented device structure as a potential and competitive candidate in the field of high-frequency and high-power applications.

Acknowledgements

The authors would like to express sincere thanks to Mr. Y. Taniguchi and Ms. M. Shojima of the Nagoya Institute of Technology, Japan, for their support during the experimental process.

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