D-7-03

Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp247-248

Effect of the Gate Width Extension in Millimeter Scale on the RF Performance of Polycrystalline Diamond MOSFETs

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Abstract

High output power performance is critical for the radio frequency (RF) amplifier applications. It is essential for diamond FETs to extend the gate width (W_G). This paper reports on the DC and RF characteristics of two-dimensional hole gas (2DHG) diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) with a total gate width extended up to 1 mm. We fabricated ALD-Al₂O₃ diamond MOSFETs which have double-finger structures with several finger lengths and evaluated the effect on performances by extending the gate width.

1. Introduction

Diamond is expected as a promising material for high-frequency and high-power amplifiers due to its excellent semiconductor properties, such as high breakdown electric field and the highest thermal conductivity. Recently, the highest output power density P_{out} = 3.8 W/mm [1] in diamond FETs was reported for ALD-Al₂O₃ diamond MOSFETs on polycrystalline diamond substrate with the double gate-finger structure (total gate width W_G = 50 μm×2). However, more than 100 W output power is desirable for the practical amplifier using diamond. Therefore, it is necessary for diamond FETs to extend the W_G. The devices with the extended finger length L_{finger} might be influenced by grain boundaries of polycrystalline diamond, self-heating, and increasing gate resistance (R_G). In this work, ALD-Al₂O₃ MOSFETs on a polycrystalline diamond were fabricated with the total gate width up to 1 mm. DC and RF performance of diamond FETs with different W_G were evaluated.

2. Device Information

Fig.1(a) shows the schematic view of ALD-Al₂O₃ diamond MOSFETs. The devices were fabricated on a type-IIa polycrystalline diamond with a (110) preferential orientation purchased from Element Six Ltd. The grain size of this substrate is about 100~300 μm [1]. The thickness of ALD-Al₂O₃ gate insulator is 100 nm. The source-gate length (L_{SG}), the gate length (L_G), and the gate-drain length (L_{GD}) were fixed to 1.0, 0.5, and 3.5 μm, respectively. W_G of the fabricated devices were 50 μm×2, 100 μm×2, 200 μm×2, 300 μm×2, 400 μm×2, and 500 μm×2, respectively. In addition, there are five devices for each W_G. Fig.1(b) and 1(c) show the top view of the fabricated devices with W_G of 100 μm and 1 mm, respectively.

3. Results and Discussion

Fig.2(a) and 2(b) have shown the drain current-voltage characteristics of devices with W_G = 100 μm and 1000 μm, respectively. The DC measurement is under the continuous wave condition, which means that the increase of the power consumption varies linearly with the extension of W_G due to the self-heating effect. At V_{GS} = −24 V and V_{DS} = −40 V, the maximum drain current density (I_{DSmax}) was −494 mA/mm for a device with W_G of 100 μm and −416 mA/mm for a device with W_G of 1 mm. However, I_{DSmax} = −494 mA/mm is the highest obtained value in this study, thus it is valuable to consider the average drain current density results of all the measured devices. Fig.3 shows the $I_{DS\,max}$ of all devices and the average $I_{DS\,max}$ of each W_G. From the approximate line obtained from these results, it was found that extending W_G from 100 μm to 1000 μm has reduced the current density by only 8%. If W_G is larger, there are more grain boundaries distributed across the active areas of devices. In addition, the self-heating effect is more obvious for the devices with larger W_G. In terms of this result, it can be confirmed that the current reduction by grain boundaries and self-heating is not severe. The small signal S- parameters were measured at the bias of V_{GS} = 16 V and V_{DS} = −40 V. Fig.4 shows the typical values of the cutoff frequencies (f_T) and the maximum oscillation frequencies (f_{max}) of the devices with different W_G. f_T and f_{max} were not de-embedded, and included the parasitic pad capacitances and inductances. No obvious degradation of f_T was confirmed when increasing W_G. The reason is that, in theory, f_T could not be affected by the increase of gate resistance R_G due to the increase of W_G. However, it can be seen that f_{max} is decreased with the increase of W_G because R_G is increased due to the extension of L_{finger}. In this device, the thickness of the gate electrode metal is as thin as 100 nm. Therefore, the reduction of f_{max} can be further suppressed by thickening the gate electrode metal.

The large signal performance was evaluated using a load pull system at 1 GHz. The bias point under A-class operation was selected at V_{GS} = 8 V and V_{DS} = −30 V. Remarkable

changes were observed under different impedance match conditions. Fig.5 shows the maximum power gain (Gain) of each W_G. For those devices with smaller W_G, which possess larger impedance, the obtained lower Gains are limited by the impedance mismatching at the source tuner. In case of the devices with larger W_G, which exhibit smaller impedance, the higher tuner impedance approaches the optimum matching impedance, thus higher gains were obtained. However, when W_G exceeded 400 μm, Gains were decreased due to the degradation of f_{max}. Therefore, the results of this work suggest that W_G of 400 μm (L_{finger} = 200 μm) is optimal to evaluate the RF performance of polycrystalline diamond FETs with thick Al_2O_3.gate insulator.

4. Conclusion

In this work, ALD-Al_2O_3 diamonds MOSFETs with W_G up to 1 mm were evaluated. Device performances such as I_{DS} and f_T, were not obviously deteriorated, while f_{max} degradation was confirmed when extending W_G. However, it can be mitigated by reducing R_G using the processes such as T-gate, the multi-finger structure, and thicker electrode metal. These results indicate that polycrystalline diamond substrates are also suitable for the amplifier application.
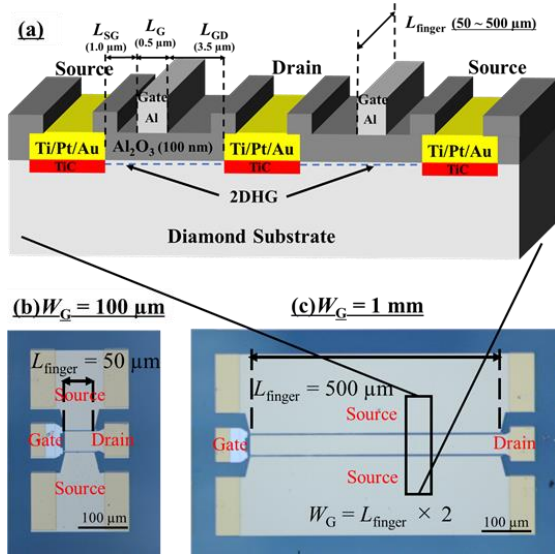

Fig.1 (a) The schematic view of ALD-Al_2O_3 diamond MOSFETs. The optical microscope views of the devices with W_G of (b) 100 μm and (c) 1 mm.
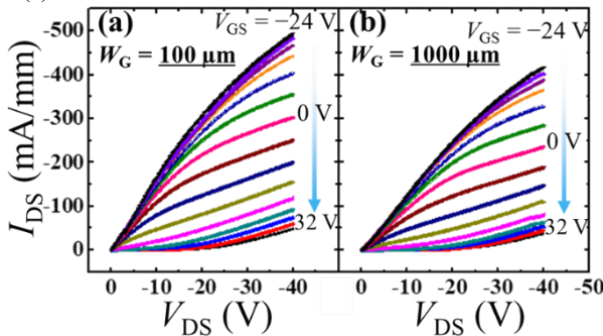

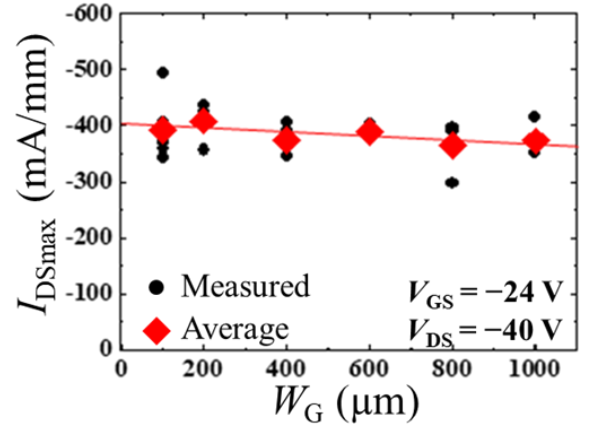Fig.2 I-V characteristics of devices with W_G = (a) 100 μm and (b) 1000 μm.

Fig.3 The measured and average I_{DSmax} scaling as a function of W_G from 100 to 1000 μm.
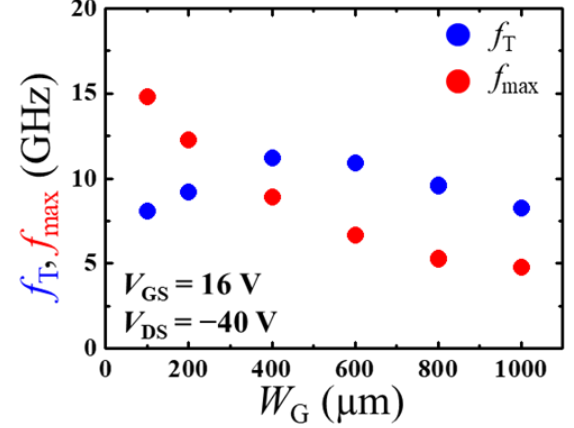

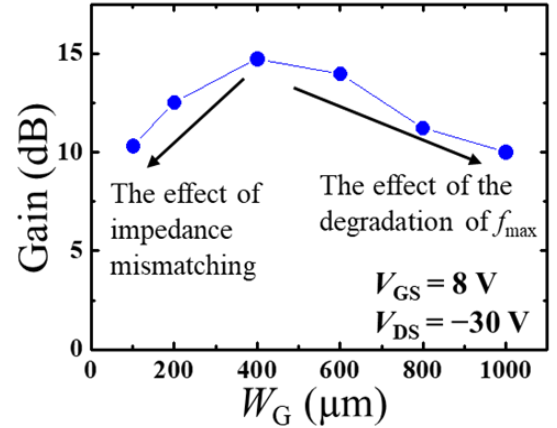Fig.4 f_T and f_{max} results scaling as a function of W_G from 100 to 1000 μm.

Fig.5 Maximum power gain obtained using a load pull system at 1 GHz scaling as a function of W_G from 100 to 1000 μm.

References

[1] S. Imanishi, H. Kawarada et al: IEEE EDL. 40 (2019) 279.