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Innovative Silicon (i-Si) Power Device with Time-Spatial Carrier Control

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Abstract

An innovative silicon power device (i-Si) is proposed that breaks through the loss limitation of conventional insulated gate bipolar transistors (IGBTs). By applying time-spatial control of a stored carrier at the state of conduction and switching of IGBT with a structure of additional control gate and divided drift combining gate driving technology, the power loss performance overcomes the trade-off between lower saturated voltage and lower turn-off loss. A proposed dual side-gate high-conductivity IGBT (HiGT) through time and space control of a stored carrier (TASC), which is a component of 6.5 kV rated i-Si, showed -40% turn-off loss from the leading-edge IGBT. Proposed i-Si can provide higher-power with low-cost solution.

1. Introduction

For more than 37 years, IGBTs have been improved in terms of reduced power dissipation with lower conductive and switching losses by various technologies such as a scaling rule for the IGBT [1] and HiGT concept [2]. Figure 1 shows the historical changes of IGBTs and an applied 3.3kV power module's inverter loss and rated currents that have the gate structures of a planer-gate [3], a trench-gate [4], and a leading-edge side-gate [5]. The conventional planar-gate and trench-gate have shown lower saturated voltage (V_{CEsat}) due to enhanced conductivity modulation at the conduction of IGBTs. Furthermore, side-gates, which have a side-wall gate structure surrounded by a thick gate oxide layer, have achieved a lower turn-off loss (E_{off}) and turn-on loss (E_{on}) due to a lower feedback capacitance (C_{res}) characteristic. However, further improvement of loss performance has reached a limitation because of the trade-off relationship between V_{CEsat} and E_{off} due to the stored carrier density at the conduction state of IGBTs. For a technology breaking through IGBT's limitation, we have proposed the concept of dynamically controlling carrier density with additional side-gate, named i-Si [6,7] using low cost silicon semiconductor. In this paper, we demonstrate the lower-loss performance of 6.5 kV rated dual side-gate HiGT through TASC (TASC HiGT) that is a component of i-Si power device.

2. Concept on Time-spatial Carrier Control

There is a trade-off relationship between V_{CEsat} and E_{off} due to stored carrier distribution caused by conductivity modulation of IGBT. Figure 2 shows the trade-off of the leading-edge side-gate HiGT. With a highly hole injection type from a high-dose p-collector, the promoted conductivity modulation at IGBT conduction generates low V_{CEsat} performance, whereas a high turn-off current generates high E_{off} at the switching. On the other hand, a lowly hole injection type shows high V_{CEsat} with low E_{off}. Therefore, to break through the limitation on IGBT losses, a method on mode control with time-spatial scale was proposed. In the conductive state of IGBT, a large amount of carriers should be stored for low V_{CEsat}, while at the right before turn-off switching, stored carrier density near the emitter surface region of the drift layer should be reduced to promote the depletion of the drift and reduce the turn-off current for low E_{off}. A combination of TASC HiGT and gate driving technology optimizes the carrier density in accordance with the states, thereby enabling drastic low-loss performance.

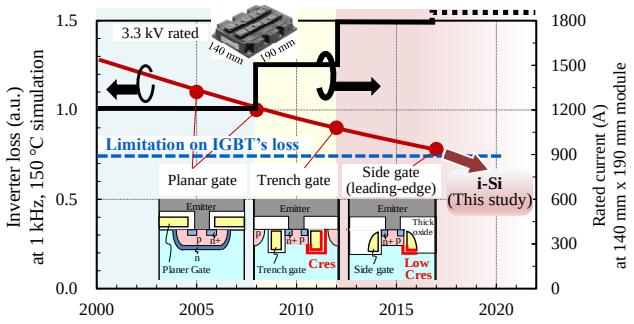

Fig. 1 Historical changes of IGBT structure and performance.

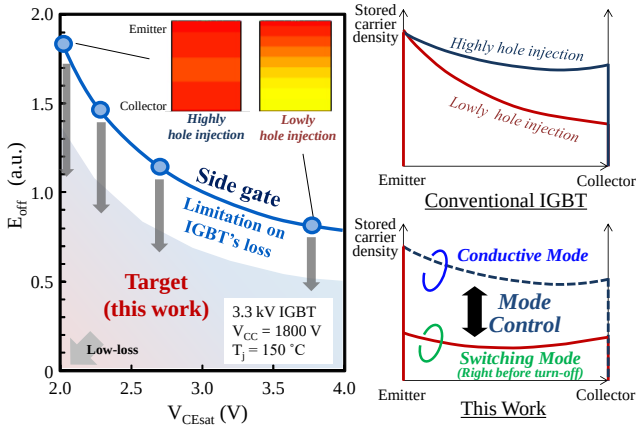

Fig. 2 Trade-off of IGBT generated by stored carrier and our target.

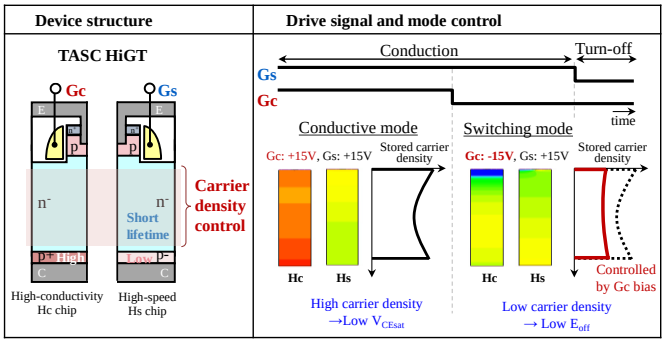

Fig. 3 Proposed structure of TASC HiGT, and applied gate driving technology.

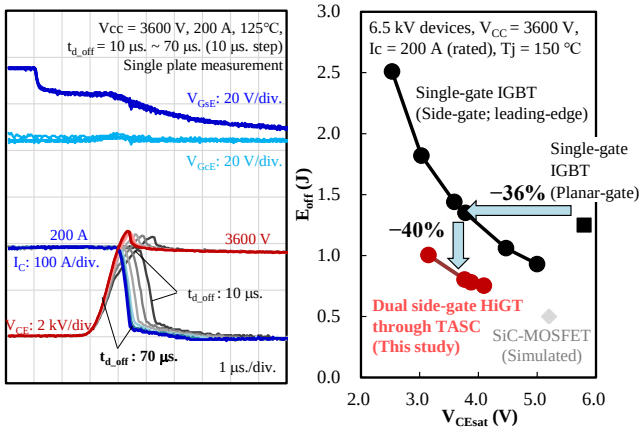

Fig. 4 Experimental turn-off waveforms of TASC HiGT with the parameter of t_{d_off}, and trade-off performances on V_{CEsat} and E_{off}.

3. Low-loss of TASC HiGT

Figure 3 shows the configuration of 6.5 kV rated TASC HiGT and gate drive technology. Our proposed TASC HiGT consists of two chips connected in parallel; one is a high-conductivity (Hc) chip with a high-dose p-collector layer, and the other is a high-speed (Hs) chip with a low-dose p-collector layer. This has two isolated gate terminals; one is a switching gate (Gs), and the other is a carrier control gate (Gc) that can control the stored carrier density during conduction and right before turn-off switching. The gate driver, converting a PWM command signal to an isolated two driving signals, are designed to switch between conduction and switching mode with timing delay of t_{d_off}. During the conduction mode of TASC HiGT, both Gs and Gc bias of +15 V inject electrons from an emitter to the drift to promote conductivity modulation in an Hc chip and obtain low V_{CEsat} performance. During the switching mode right before turn-off, the preceding Gc bias of -15 V extracts the hole carriers from a Hc chip, moves them to a Hs chip to suppress conductivity modulation, and then creates the fast switching profile. This is the time-spatial carrier control that enables higher controllability of stored carrier density [7]. Figure 4 shows the experimental turn-off current, voltage waveforms, and trade-off of a TASC HiGT. By setting t_{d_off} longer, lower stored carrier density creates the lower turn-off tail current leading to lower E_{off}. Considering the temporary conduction loss increase at the period of t_{d_off}, 65 µs. is the optimal driving parameter. TASC HiGT shows -40% lower E_{off} than the leading-edge side-gate HiGT, maintaining low V_{CEsat} of 3.7 V. Breaking thorough the loss limitation of 6.5 kV IGBT could be demonstrated with the proposed TASC HiGT. Proposed carrier control concept could also be applied to a freewheeling diode (FWD), named MOS controllable stored-carrier diode (MOSD) [7]. Our i-Si, which is composed of TASC HiGT, MOSD, and their driving technology, can provide a low-loss and high-power module with low-cost for innovative power semiconductor devices.

4. Conclusions

In this paper, i-Si power device technology with time-spatial carrier control concept was proposed for breaking through the conventional IGBT loss limitation. TASC HiGT with gate driving technology can optimize the stored carrier density at the state of conduction and right before switching. Experimental results show -40% lower E_{off} from the leading-edge side-gate HiGT, maintaining low V_{CEsat} performance, breaking through the conventional trade-off of IGBT. The feasibility of the innovative low-loss and low-cost Si solution was demonstrated.

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