Experimental Demonstration of Bileg Silicon-nanowire Thermoelectric Generator with Cavity-free Structure

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Abstract

This work is the first experimental demonstration of a bileg Si-nanowire (Si-NW) micro thermoelectric generetor (TEG) with cavity-free architecture for designing a large scaled integarated planar Si-NW TEG. In the bileg-TEG, the mobility and thermopower mismatches between electron and hole effects on the optimum dimensional parameters of n- and p-type Si-NWs and optimum dose of impurity. In this work, under a specific dose condition, we explored the optimum ratio of NW width of n- and p-type Si-NWs. We compared our experimental data with equivalent circuit model. The results of the wire width dependency of the power generation gives a fundamental guide for designing integrated planar Si-NW TEG module.

1. Introduction

The modern world's demand for huge power generation to develop new materials and technologies. Thermoelectric conversion of heat to electricity plays an important role to produce power generation. Thermoelectric devices such as TEG have definite advantages. They have no moving parts, and barring accidents or thermal deterioration. TEGs consist of a set of thermoelectric (TE) modules inserted between two heat exchangers.

Recently, we proposed a planar Si-NW TEG with cavity-free architecture, that is more fruitful than conventional TEG [1-3]. In the cavity-free TEG, the TE power generated from a unit area is enhanced by shrinking the length of Si-NW by applying a steep temperature gradient in each NWs. TEGs are categorized into two groups: unileg- and bileg-TEGs. A bileg TEG is composed both of n- or p-type semiconductors, and the bileg-TEG become simple structure than the unileg-TEG. However, to fabricate high performance the bileg-TEG, the mobility mismatch between electrons and holes of Si semiconductor should be considered to achieve impedance matching between n- and p-type semiconductors by adjusting the widths of both types of Si-NWs.

In this work, we evaluate the fundamental dependence of the TE performance on the width of the p-type Si-NWs under a dose condition, to design the high performance micro bileg-TEG in future.

2. Experimental

The cavity-free planar TEG is fabricated on an SOI substrate, as shown schematically in Fig. 1. The thicknesses of the Si-substrate, the BOX layer, and the top SOI layer were 745 μm, 145 nm, and 50 nm, respectively. The SOI layer was patterned into Si-NWs with a width less than 120 nm. Phosphorus ions (dose 9.0×10^{14} ions/cm^2) were implanted at an acceleration energy of 20 keV for n-type region. Boron difluoride ions (dose 8.0×10^{14} ions/cm^2) were implanted at an acceleration energy of 30 keV for p-type region. The implantation was followed by activation annealing at 1000 °C. A single device comprised a 100-lines Si-NW bundle with a pitch of 500 nm. The length of the Si-NWs is 10 μm. Both the ends of a Si-NW bundle were connected to separate Si pads. These Si-NWs and Si pads were wrapped in a thin SiO$_2$ film. Next, this SiO$_2$ layer at the Si pad regions was removed. A 400 nm-thick Al/TiN/Ti was deposited on the Si pad as the electrode. We connected the hot and hot side of N-and p-type TEG by 5 μm-wide Al wire in series.

The TE power was measured by externally applying a temperature difference ΔT_{ext} between surface and bottom of the specimen. The hot-side electrode was heated by attaching a micro-thermostat, whose temperature is maintained at 33, 38 or 43 °C. The base stage beneath the substrate was maintained at 23 °C by a Peltier cooler. The heat current flowed perpendicularly to the Si substrate and partially exuded in the horizontal direction. The exuded heat current formed a steep temperature gradient in the proximity of the heat source, thereby inducing a TE current through the Si-NWs.

3. Results and Discussion

We measured the electrical resistance, open circuit voltage (Voc) and TE power of different width of NWs at the various temperature. The dependence of the open circuit voltage on the external temperature difference became a linear slope in our experiment as shown in Fig. 2a. The linear slope is proportional to Seebeck coefficient. The TE power is proportional to external ΔT^2 as shown in Fig. 2b.

As shown in Fig. 3, the slope of p-type NW is about two times larger than the that of n-type NW. The measured internal resistance is shown in the Fig.4.

TE power normalized by the total footprint of the NW bundle excluding the Si-pad area (Fig. 5). In the fabricated TEG, the length of Si-NWs and the pitch between each Si-NWs are fixed. Therefore, the TE power is expected to depend on the polarity of NW (n- or p-type) and the width of each NW. The experimental result shows, the areal power density of the p-type leg varied with the NW width. The width dependency can be explained by the difference in the Seebeck coefficients depending on the NW width, which is shown in Fig. 3. In the previous work [4], it was pointed out that the Seebeck coefficient of Si-NW is affected by the surface charges on the Si-NWs. If negative charges are fixed at the Si-NW surface, the Seebeck coefficient is shift toward positive side. Therefore, the Seebeck coefficient will be deteriorated in n-type NW and enhanced in p-type, and the extent will depend on the NW width.

TE power of the bileg-TEG as a function of the width of p-type Si-NW evaluated at ΔT_{ext} = 20 K (Fig. 6). Solid curve is the numerical estimate with the equivalent circuit model shown in Fig. 7 [3]. θ_{NW} and θ_{sub} are the thermal resistances

of the Si-NW and the Si substrate, respectively. $\theta_{SiO_2}^{\perp}$ and $\theta_{SiO_2}^{//}$ are vertical and horizontal components of the thermal resistances of the BOX layer, respectively. V_{oc} is the measured open-circuit voltage appearing at both ends of a Si-NW, and R is the measured electrical resistance. The assumed parameters of heat conductivity, κ, electrical resistivity, ρ, and Seebeck coefficient, S, are summarized in TABLE I. In the present experiment, the optimum width of the p-type is predicted to be 76 nm when the n-type width is 60 nm. The experimental result agreeing with the calculation.

4. Conclusions

We fabricated a bileg Si-NW TEG with our proposed cavity-free planar device architecture. We evaluated the device resistance, open circuit voltage and generation power of different width of Si-NW applying external temperature difference successfully. The equivalent circuit of the bileg TEG with the evaluated parameters could give a fundamental guide for designing integrated planar Si-NW TEG module.

References

[1] T. Watanabe *et. al.*, IEEE EDTM Proc. Tech. Papers, (2017) 86.
[2] H. Zhang *et. al.*, IEEE Trans. Electron Devices **65** (2018) 2016.
[3] M. Tomita *et. al.*, IEEE Trans. Electron Devices **65** (2018) 5180.
[4] S. Hashimoto *et. al.*, Appl. Phys. Lett. **111** (2017) 023105.

TABLE I
Parameters used in equivalent-circuit model.

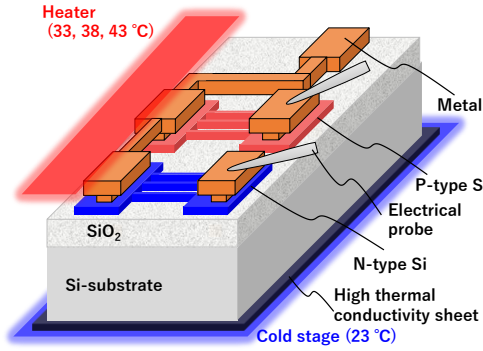| Parameter		Parameter	
κ_{NW}	16.4 W/mK	κ_{sub}	131 W/mK
κ_{SiO2}	1.4 W/mK		
S (n-type)	-60 µV/K	ρ_{NW} (n-type)	4.2×10^{-3} Ωcm
S (p-type)	40 µV/K	ρ_{NW} (p-type)	5.5×10^{-3} Ωcm

Fig. 1. Schematic of fabricated TE generator. n- and p-type components can be measured separately by the ternary electrode.
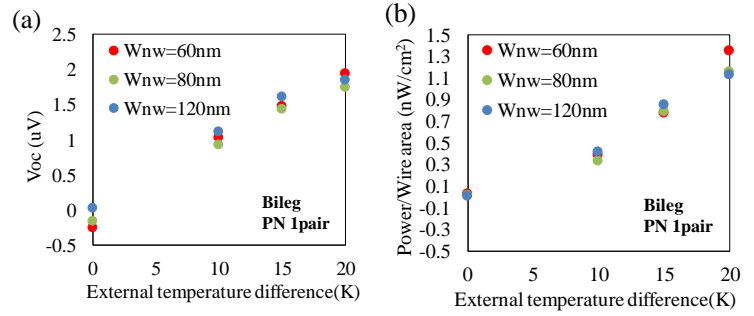

Fig. 2. (a) Open circuit voltage and (b) Power/ Wire area at external temperature difference for 1 pair bileg p-type NW.
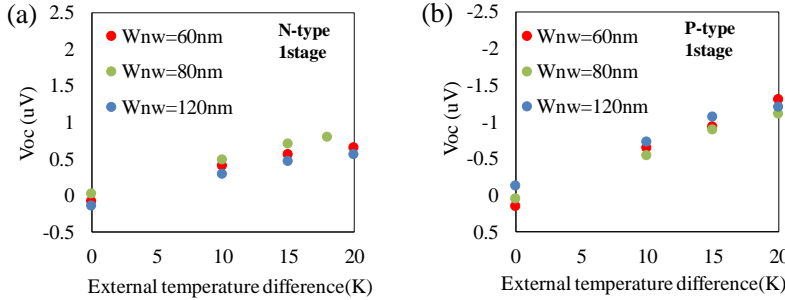

Fig. 3. Open circuit voltage on external temperature difference for (a) n-type and (b) p-type NW in the Experiment.
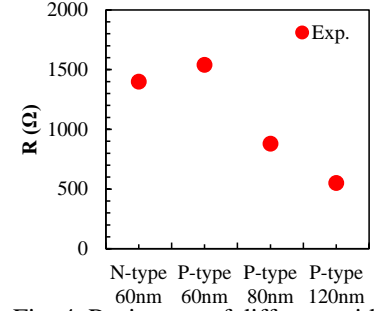

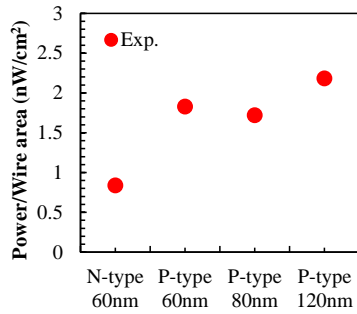Fig. 4. Resistance of different width of n- and p-type NW in the experiment.

Fig. 5. Areal power densities of different width of n- and p-type NWs at $\Delta T_{ext} =$ 20 K.
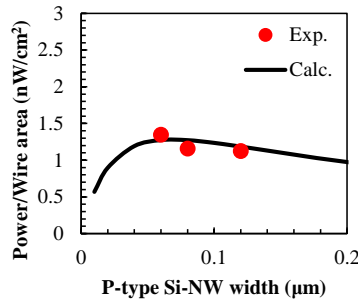

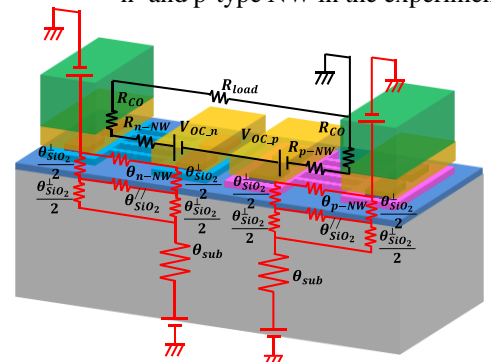Fig. 6. Areal power density of bileg TEG vs width of p- type Si-NW.

Fig. 7. Schematic of equivalent circuit model of the bileg TEG.