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Estimation of Seebeck Coefficient of Si Wire Laterally Lying on Oxide-Covered Substrate

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Abstract

We characterized the Seebeck coefficient of Si wires formed on an oxide-covered substrate, which is an essential component of a proposed planar-type micro thermoelectric (TE) generator. The Si wires are laterally lying on the oxide-covered substrate, so that the injected heat current leaks out from the Si wires to the substrate. Nevertheless, the Seebeck coefficient of the Si wires was not so deteriorated from a nearly adiabatic case where Si wires are suspended in air.

1. Introduction

Towards the IoT society, TE generator is attracting many attentions as a permanent power source for distributed sensor nodes. Si-based TE generator is one of the expected power sources because they are manufacturable using Si CMOS process [1].

Recently, we proposed a cavity-free planar TE generator with using Si wires which are fabricated on an SiO_2/Si substrate. In this device architecture, as shown in Fig. 1, most of the heat current injected into the Si wires leak out toward the substrate, thereby the temperature profile in the Si wires no longer render a linear gradient [2]. Although the heat leakage seems unfavorable to exploit the TE ability, it is not certain that the Seebeck coefficient is effectively deteriorated in the Si wires laterally lying on the substrate. Here, the effective Seebeck coefficient is defined as the open-circuit output voltage divided by the temperature difference between both ends.

In this study, we estimated the effective Seebeck coefficient of Si wires formed directly on an SiO_2/Si substrate. The precise temperature difference across the Si wire was estimated by metal wire resistance thermometers formed at both ends of the Si wires.

2. Experimental

The effective Seebeck coefficient of Si wires was evaluated by varying the number of wires, the width, and the spaces between each wire.

The Si wire samples were prepared by the following processes. First, a p-type Si (100) SOI substrate (SOI: 88 nm, BOX: 145 nm, Si-substrate: 745 μm) was patterned by electron beam lithography and reactive ion etching, and a thermal oxide film about 20 nm was formed on the surface. Subsequently, P^+ ions were implanted at dose of 1.0×10^{15} cm^{-2} and acceleration energy of 25 keV, and activation annealing (950 °C, 10 min) was performed. The thickness and active impurity concentration of the Si wires were about 70 nm and 7×10^{19} cm^{-3}, respectively. Finally, metal films (Ti: 10 nm, TiN: 30 nm, Al: 400 nm) were deposited by sputtering to form electrodes and resistance thermometers which measures the temperature difference between both ends of the Si wires (ΔT_{wire}). Then, a forming gas annealing (FGA) was conducted to the samples whose spaces between each wire were varied. We prepared three different numbers of Si wires (5, 20, and 100), two different widths (0.5 and 2.0 μm), and four different spaces between each wire (0.5, 1.0, 2.0 and 10 μm). The Si wire length is set to 3.0 mm.

Fig. 2 shows the schematic of TE generators. For the calibration of the resistance thermometers, the stage temperature was changed from 20 °C to 40 °C to measure the temperature coefficients of the resistance thermometers. The temperature coefficients of metal wire samples with and without FGA were about 0.330%/K and 0.341%/K, respectively. Upon the TE power measurement, a micro heater was pressed on the hot side electrode of the TE generator. The temperature difference between the micro heater and the stage was kept at 15 K. The ΔT_{wire} was determined by measuring the resistance of thermometers. Finally, the open-circuit output voltage (V_{oc}) of the TE generator was measured by a nano-volt meter to estimate the Seebeck coefficient.

3. Results and Discussion

The measurement results of the ΔT_{wire} and the V_{oc} are summarized in Fig. 3. The horizontal axis is the ΔT_{wire}. Although the externally applied temperature difference between the micro heater and the stage is kept constant at 15 K, the contact thermal resistance between the sample and hot/cold sources varied from measurement to measurement. Therefore, the ΔT_{wire} was changed for each measurement.

Clear proportional relationships appear between the ΔT_{wire} and the V_{oc} in Fig 3(a), (b) and (c). The Seebeck coefficient was estimated to be approximately −170 μV/K. In literature, the Seebeck coefficient of the SOI layer is reported to be −500 μV/K at an impurity concentration of $5\times10^{19}$$cm^{-3}$ [3]. A simulation ignoring phonon drag effect estimated the Seebeck coefficient to be −130 μV/K at an impurity concentration of 7×10^{19} cm^{-3} [3]. Present result is very closer to the simulation result, but the coincidence does not necessarily substantiate the vanishing of the phonon drag, because the Si wires used in this work is wide enough to compare the SOI film thickness. Anyway, the effective Seebeck coefficient estimated in this work is similar in the order of the previous report.

As shown in Fig. 3(a), there is no meaningful difference in the distribution of the ΔT_{wire} for different number of Si wires, in spite that the thermal resistance of the Si wires differs by 20 times. The result shows that the thermal resistance of the Si wires is negligible in our device. This is because that most of the heat current flow into the substrate and only small portion of heat current spreads into Si wires to establish the

temperature gradient [2].

For the same reason, the width and the space do not affect the temperature difference across the Si wires as shown in Fig. 3(b) and (c). The effect of the space between each wire on the TE performance was not observed in our previous work [4].

It was reported that the FGA is effective to suppress an anomalous change in the Seebeck coefficient of thin Si wires with 45 nm [5]. However, as shown in Fig. 3(c), there is no significant change in Seebeck coefficient before and after FGA. This is considered due to the difference in the Si wires; present work employs 0.5 and 2.0 μm-wide Si wires, which are much wider than the previous report [5].

In our device architecture, width of Si wire is found to be unessential to enhance the TE performance, so that the Si wires can be replaced with wide Si membrane.

4. Conclusions

We estimate the Seebeck coefficient of Si wire laterally lying on SiO_2/Si substrate. The clear proportional relationships between the temperature differences and the TE voltages is obtained by using metal wire resistance thermometers. The effective Seebeck coefficients was not deteriorated much compared to the reported value [3]. Therefore, it is found that our proposed cavity-free planar TE generator has the potential for enough TE performance. It is future work to evaluate effective Seebeck coefficient of short Si wires on SiO_2/Si substrate.

Acknowledgements

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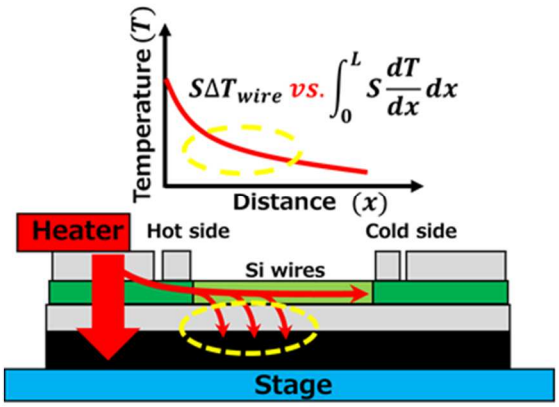

Fig. 1 Heat current illustration in cavity-free structure.

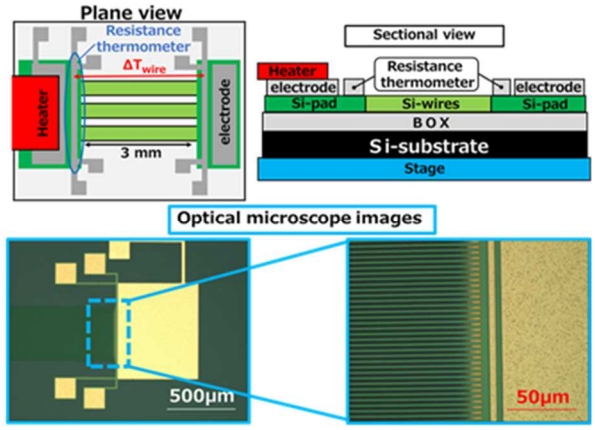

Fig. 2 Schematic views of TE generators.

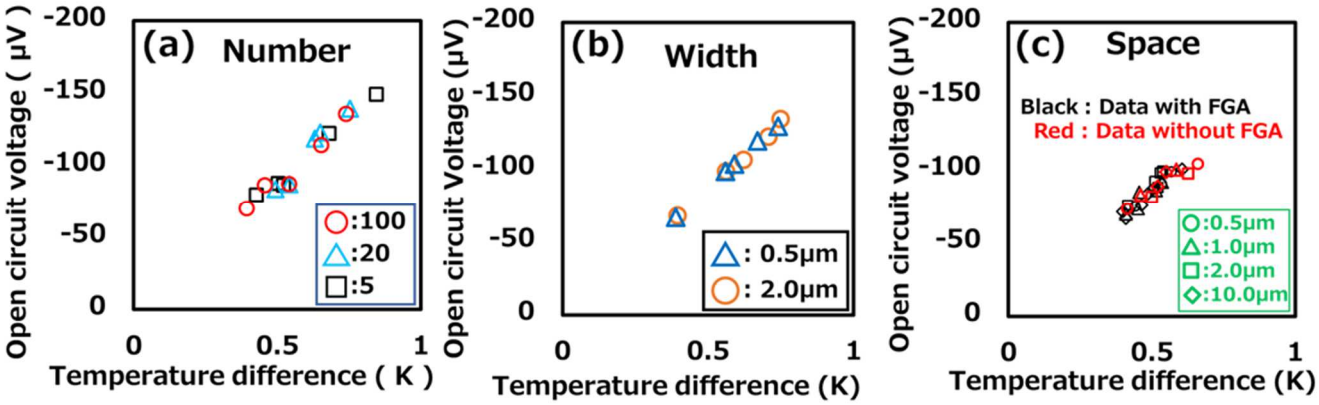

Fig. 3 ΔT_{wire} vs. V_{oc} obtained by metal wire resistance thermometers. (a) the devices with 5, 20, and 100 parallel Si wires when width and space are 2 μm. (b) the devices with 0.5 μm-wide 40-parallel Si wires and 2.0 μm-wide 10-parallel Si wires when space is 2.0 μm. (c) the devices with Si wire spaces of 0.5, 1.0, 2.0, and 10 μm when width and number are 2.0 μm and 50, respectively. The Si wire length is set to 3.0 mm.