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Quantification of Insulator and Semiconductor Carrier Trapping in Organic Thin Film Transistors Using DNTT and TU-1

Kunihiro Oshima,[1] Kazunori Kuribara,[2] Song Bian,[1] and Takashi Sato[1]
[1] Graduate School of Informatics, Kyoto University Yoshida-hon-machi, Sakyo, Kyoto 606-8501, Japan
Phone: +81-75-753-4983 E-mail: paper@easter.kuee.kyoto-u.ac.jp
[2] National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Higashi, Tsukuba, Ibaraki 305-8565, Japan

***Abstract*—We propose a measurement based quantification of the insulator trapping and the semiconductor carrier trapping upon $V_{\rm th}$ degradation of organic thin film transitors. We propose and use a bias-stress degradation model that is composed of the above two trapping terms. Through the determination of its parameters based on measurement results, insulator and semiconductor trapping components are quantified considering bias-stress voltage.**

1. Introduction

Organic thin film transistors (OTFTs) can be manufactured on flexible, large-area substrates by printing or spin-coating processes. They are promising devices that facilitate new area of applications such as flexible sensors for wearable devices [1-3]. At present, relatively fast performance degradation of OTFTs is limiting their applications. The degradation is explained mainly by two mechanisms: the reaction of semiconductor with oxygen or moisture in air, and the bias-stress induced carrier trapping at insulator or semiconductor [4]. The former is relatively easy to suppress by the encapsulants [5], while the latter is difficult because the bias voltage that are applied during the normal operation of the OTFTs causes the degradation.

In this paper, we experimentally study the components of bias-stress induced carrier trappings in OTFTs. Ref. [6] reported that semiconductor carrier trapping (SCT) is a dominant factor in the degradation of p-type OTFTs when applying bias stress. However, it is difficult to separate contributions of the SCT and insulator carrier trapping (ICT). Such technique would be useful to identify the cause of the rapid bias-stress induced degradation in OTFTs. We hence propose a novel degradation model for OTFTs consisting of ICT and SCT terms. Through the parameter fitting of the proposed model, the contribution of the trapping components on a measurement result is studied.

2. Measurement setup

The OTFTs of a bottom-gate and top-contact structure shown in Fig. 1 were fabricated as DNTT and TU-1 the semiconductor materials. The measurement consists of two steps: (i) measure $I_{\rm D}$-$V_{\rm GS}$ curve at $V_{\rm DS}=3.0$ V, and (ii) apply bias-stress voltage ($V_{\rm GS}$) for 30 seconds. We repeat steps (i) and (ii) alternatively. The different bias-stress voltages are applied for five OTFTs, $V_{\rm GS}=0.0$ V, 1.5 V, 2.0 V, 2.5 V, and 3.0 V, where $V_{\rm DS}=0.0$ V. Note that the condition $V_{\rm GS}=0.0$ V represents the degradation caused by the $I_{\rm D}$-$V_{\rm GS}$ curve measurement only. All measurements are carried out in room temperature.

3. Analysis of bias voltage dependent degradation

We propose a novel bias-stress degradation model as:

$$\Delta V_{\rm th}=r\ln\left(1+\frac{t}{q}\right)+\Delta V_{\rm semi}(\infty)\left(1-\exp[-(\frac{t}{\tau})^s]\right). \quad (1)$$

$\Delta V_{\rm th}$ represents the change of threshold voltage. The first term in the proposed model represents the ICT [7-9] and the second term represents the SCT [6,10], assuming that the trapping rate and trapped carrier distribution are mutually independent. Here, r and q determine the magnitude and the degradation rate due to ICT, respectively. $\Delta V_{\rm semi}$ represents the saturation value of threshold voltage shift, and s and τ govern the degradation rate due to SCT.

In order to quantify the insulator and the semiconductor trappings, we fit the model equation to the measurement results as shown in Fig. 2. In (a), r can be derived as the slope of Eq. (1) on a semi-log plot after a long stress time, where $t \gg q$ and $(1-\exp[-(t/\tau)^s]) \approx 1$. In (b), for the same time range, by determining the slope and the intercept of taking the exponential of Eq. (1), we find q and $\Delta V_{\rm semi}(\infty)$. In (c), we find s and τ by calculating the slope and the intercept of the logarithm of the same equation for shorter stress time range.

Fig. 3 shows the model-fitting results of $\Delta V_{\rm th}$ and the contributions of the ICT and SCT at different bias voltages. Fig. 4 shows the total $V_{\rm th}$ degradation of ICT and SCT after approximately 15000 seconds. Larger degradation is found as the stress voltage becomes higher. Degradation due to ICT in n-type is 10x larger than that in p-type OTFT. It implies that the ICT is the major cause of the rapid degradation of n-type OTFTs, though the oxidation of the Al gate, etc., may additionally be the causes.

In Figs. 3(c) and (d), we observed the long term fitting error, so we additionally carried out longer measurements for these conditions. As shown in Fig. 5, $V_{\rm th}$ saturates at the similar values regardless of the applied stress voltages. Bias-stress degradation by SCT, which is dominant in Figs. 3(c) and (d), depends on the stress voltage, and is more pronounced when oxygen or moisture penetrates into organic semiconductors [10], which we guess one reason of the relatively large $V_{\rm GS}$ dependent $V_{\rm th}$ shift. In order to improve the fitting accuracy, measurements in dry and low-oxygen environment would be necessary. Considering the different $V_{\rm th}$ convergence rates between the applied stress voltage, Joule heating may also be involved. We would like to leave this as our future work.

4. Conclusion

Contributions of the trap locations in the degradation of OTFT are quantified through the fitting of the proposed bias-stress degradation model to the measured $V_{\rm th}$ change. The

experiments have shown quantitative changes of ICT and SCT for different bias stress voltages, and the rapid degradation of the n-type OTFTs is mainly attributed to the ICT.

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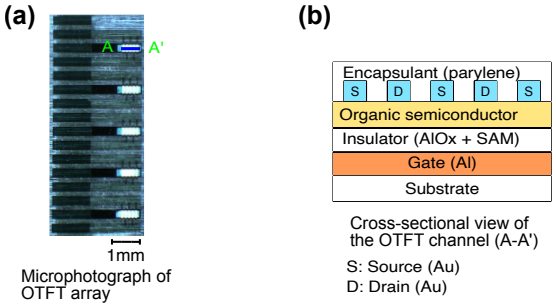

Fig. 1: Layout of the measured five bottom-gate and top-contact OTFTs (a) and the cross section of OTFT (b). The organic semiconductor materials are TU-1 and DNTT for n- and p-type OTFTs, respectively. The insulator thickness is 4 nm for AlO_x and 2 nm for self-assembled monolayer (SAM), and that of semiconductor layer is 30 nm. The channel length and width of the OTFTs are 20 μm and 2000 μm, respectively.

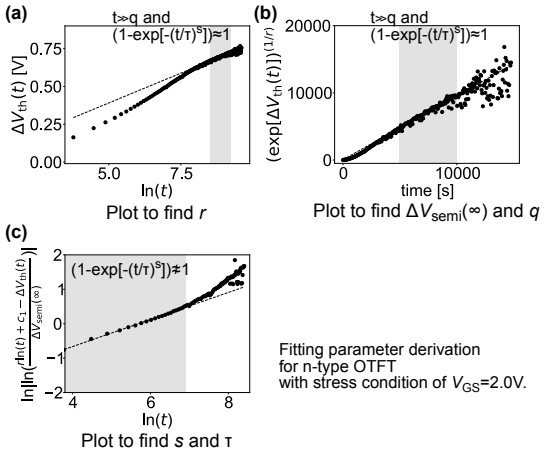

Fig. 2: Fitting parameter derivation of the proposed model. Symbols represent measurements and broken lines are Eq. (1). Least-square fitting is carried out for the data in highlighted time range. The slopes and the intercepts are used for fitting the parameters. Note that the time ranges for fitting are different among stress voltages and n-type or p-type.

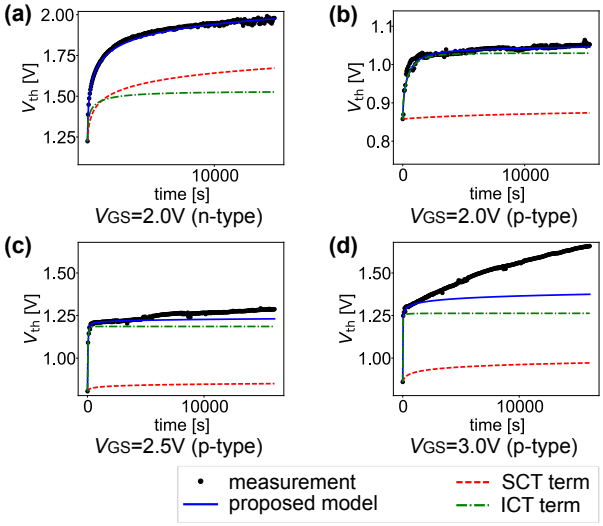

Fig. 3: Model fitting of threshold voltage (V_{th}) degradation. The model matches well with the measurements for most of the cases (such as (a) and (b)) except for the high stress voltage cases ((c) and (d)).

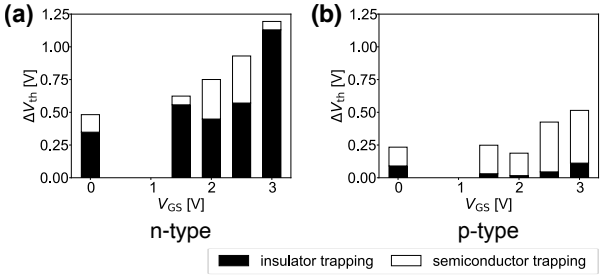

Fig. 4: Total V_{th} shifts and the breakdown of the cause at approx. 15000 seconds measurements. The average total degradation of each trapping components is 0.61 V about n-type insulator trapping, 0.19 V about n-type semiconductor trapping, 0.016 V about p-type insulator trapping, and 0.17 V about p-type semiconductor trapping. The SCT induced V_{th} shifts are almost same in n-type and p-type, but the ICT induced V_{th} shifts in n-type is 10x larger than p-type.

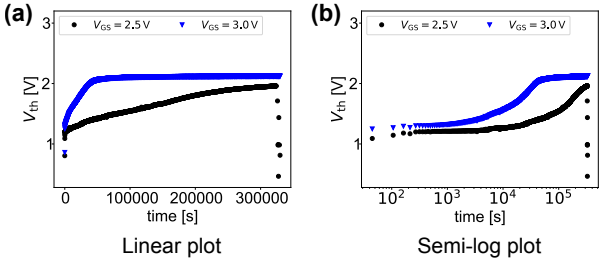

Fig. 5: Measured long term V_{th} shift of p-type OTFT. The total measurement time is about 83 hours. The same convergence values regardless of applied stress voltage indicate that the long-time scale V_{th} shifting does not owe to applied stress voltage but another degradation factor such as reaction of organic semiconductor and oxygen or moisture in air.