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Low Contact Resistance between Sputtered-MoS_2 and Self-Aligned-$TiSi_2$ Films Treated by Higher-Temperature Forming-Gas Annealing

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Abstract

Self-aligned-$TiSi_2$ contacts to sputtered-MoS_2 films are investigated, because $TiSi_2$ films have low work function and chemical stability. Owing to a higher-temperature forming-gas anneal, a low contact resistivity of 1.72 x 10^{-4} Ω-cm^2 with the $TiSi_2$ contacts to the MoS_2 films was obtained with higher process-integration ability to logic LSI applications.

Introduction

Molybdenum disulfide (MoS_2) is an attractive material for future MOSFET channel, because of the remarkable mechanical and electrical characteristics such as atomically thin layer structure and high mobility of 700 cm^2/Vs [1,2]. In various methods of MoS_2 film syntheses [1-3], we focused on the sputtering method, because it has been reported that a large, uniform and low-carrier-density MoS_2 film was obtained [4]. For MoS_2 device applications, contact resistances are required to be reduced. It has been reported the low-contact resistance was obtained by low work-function metals such as scandium, molybdenum (Mo) and titanium (Ti) owing to low Schottky barrier heights against n-type MoS_2 film [2,5,6]. However, there has been a problem for pre-cleaning before MoS_2 deposition in bottom contact structure. It is certain that the chemical stability in the RCA cleaning is preserved by using a $MoSi_2$ contact underneath the MoS_2 film. However, a contact resistance of MoS_2/$MoSi_2$ stacks was still high as 2.6 x 10^{-2} Ω-cm^2 [7]. In contrast, a titanium disilicide ($TiSi_2$) film has the low work function as small as a Ti film [8]. Therefore, it is speculated that MoS_2/$TiSi_2$ contacts realize the low contact resistance, because of low Schottky barrier heights in the MoS_2 film.

In this study, we investigated on self-aligned-$TiSi_2$ contact characteristics to the sputtered-MoS_2 film for logic LSIs.

Experimental Methods

In Figs. 1, 2 and 3, a process flow, schematic image and top view of a sputtered MoS_2 channel device are shown, respectively. In this study, the Transmission Line Model (TLM) devices were fabricated in order to extract the contact resistance. An n-doped poly-Si/SiO_2/Si substrate was used and etched by the Chemical Dry Etching (CDE). After Sulfuric hydrogen Peroxide Mixture (SPM) cleaning and Diluted Hydrogen Fluoride (DHF) treatment, Ti and titanium nitride (TiN) films were deposited. Then, a self-aligned-$TiSi_2$ film was synthesized by sintering in Ar gas and Ammonia hydrogen Peroxide Mixture (APM) removal was applied as a selective etching of residual TiN/Ti films and the $TiSi_2$ surface cleaning, simultaneously. A 3-nm MoS_2 film was sputtered, and an Al_2O_3 film was directly deposited as a passivation film by the Atomic Layer Deposition (ALD) method [9]. A device isolation for the MoS_2 active area was conducted by the photolithography and the Reactive Ion Etching (RIE). After a resist removal by O_2 plasma, a forming gas (FG) annealing at various temperatures in N_2 gas with 3% H_2 was applied.

Results and Discussion

In Fig. 4, I-V characteristics are shown, and the Ohmic contacts are obtained between 500-650ºC. In Fig. 5, current values at V = 1 V on various FG annealing temperatures up to 800ºC. The maximum currents are obtained at 650ºC. On the other hand, in Fig. 6, the sheet resistances of the MoS_2 films decrease with an increase in temperature up to 800ºC. It is speculated that mobility was remarkably enhanced with slight reduction of carrier density by the high temperature annealing [10].

In Fig. 7, contact resistivities at the interface between MoS_2 and $TiSi_2$ films depending on FG anneal temperatures calculated by TLM measurements are shown with reported data [5-7,11]. In the region up to 650ºC, contact resistivities decrease with an increase in the temperature. It is speculated that alloying was enhanced by FG annealing at the interface between MoS_2 and $TiSi_2$ films. On the other hand, the contact resistance increases with an increase temperature above 650ºC. It is speculated that C54-$TiSi_2$ film agglomerations were occurred [12]. As a result, the lowest contact resistivity of 1.72 x 10^{-4} Ω-cm^2 in this study was obtained by the FG anneal at 650ºC. Low contact resistivity at the interface between the MoS_2 and $TiSi_2$ films is achieved with smaller value than that of the $MoSi_2$ film. Eventually, the MoS_2/$TiSi_2$ contact simultaneously realizes low contact resistivity and high chemical stability for MOSFET integration.

Conclusions

Low contact resistivity of 1.72 x 10^{-4} Ω-cm^2 was obtained at the interface between sputtered-MoS_2 and self-aligned-$TiSi_2$ films. Furthermore, the chemical stability was also realized at the same time. The $TiSi_2$ contact to the MoS_2 film is expected to be applied for logic LSIs.

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References

[1]B. Radisavljevic, *et al.*, Nat. Nanotechnol. 6.3 (2011) 147.
[2]S. Das, *et al.*, Nano Lett. 13.1 (2013) 100-105.
[3]Y. H. Lee, *et al.*, Adv. Mater. 24.17 (2012) 2320-2325.

[4]T. Ohashi, *et al.*, Jpn. J. Appl. Phys. 54.4S (2015) 04DN08.
[5]J. Kang, *et al.*, Appl. Phys. Lett. 104.9 (2014) 093106.
[6]M. Toyama, *et al.*, Jpn. J. Appl. Phys. 57.7S2 (2018) 07MA04.
[7]K. Matsuura, Tokyo Tech, Doctoral Thesis (2020).
[8]E. Bucher, *et al.*, Appl. Phys. A 40.2 (1986) 71-77.
[9]H. Tanigawa, *et al.*, Jpn. J. Appl. Phys. 59.SM (2020) SMMC01.
[10]M. Y. Yin, *et al.*, J. Semicond. Technol. Sci. 18.2 (2018) 153-159.
[11]E. Gourmelon, *et al.*, J. Appl. Phys. 87.3 (2000) 1182.
[12]G. E. Georgiou, *et al.*, J. Electrochem. Soc. 141.5 (1994) 1351.

- **n-doped poly-Si (120 nm)/SiO_2 (100 nm)/Si**
- **SPM cleaning and DHF treatment**
- **Photolithography**
- **Poly-Si etching by CDE**
- **Resist removal by acetone and ethanol**
- **SPM cleaning and DHF treatment**
- **Ti sputtering**
- **TiN sputtering for cap**
- **$TiSi_2$ formation (680°C, 20 sec, Ar gas)**
- **APM cleaning for residual TiN/Ti removal**
- **MoS_2 sputtering (3 nm, 400°C)**
- **Al_2O_3 passivation by ALD (15 nm, 300°C)**
- **MoS_2-active-definition photolithography**
- **Al_2O_3 and MoS_2 etching by RIE**
- **Resist removal by O_2 plasma**
- **FG (3% H_2 in N_2) annealing up to 800°C for 1 min**

Fig. 1 Process flow for TLM devices.

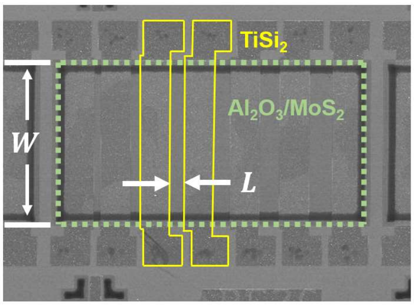

Fig. 3 Top view of the TLM device using sputtered-MoS_2 thin channel with length between contacts of 11-38 μm, width of 247 μm.

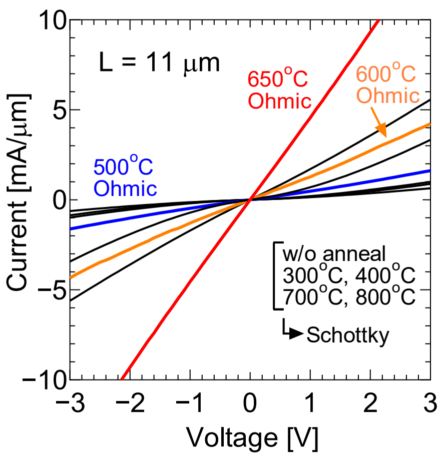

Fig. 4 I-V characteristics at various FG anneal temperatures. Ohmic contacts are observed at 500, 600 and 650°C.

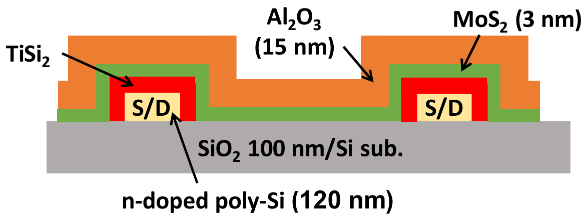

Fig. 2 Cross-sectional schematic image of the MoS_2 channel TLM device structure with the $TiSi_2$ contact.

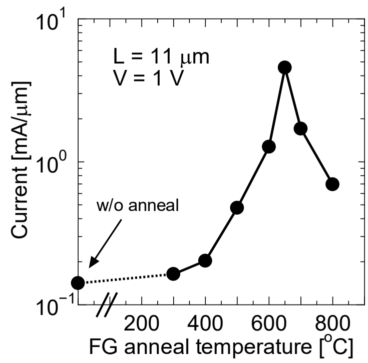

Fig. 5 Current at V=1 V depending on FG anneal temperature. The highest current is observed at 650°C.

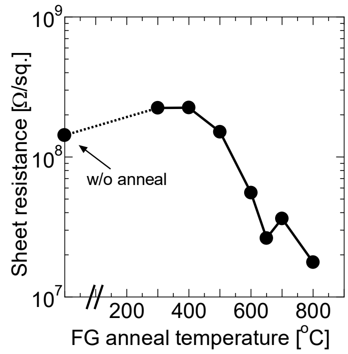

Fig. 6 Sheet resistance of the MoS_2 film underneath the Al_2O_3 passivation film depending on FG anneal temperature.

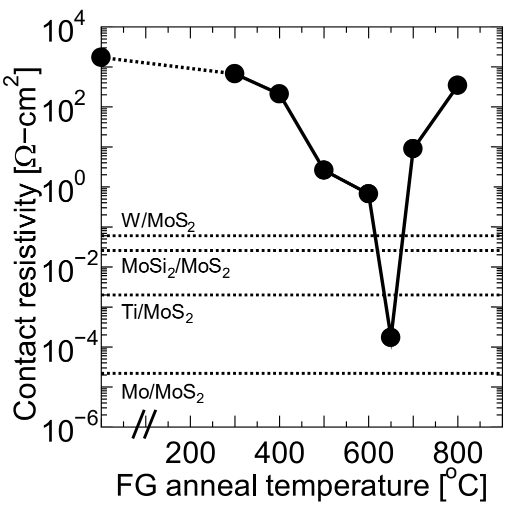

Fig. 7 Contact resistivity at MoS_2/$TiSi_2$ interface depending on FG anneal temperature and reported data with various contact metals [5-7,11].