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Carrier density of apparently degenerated PtS_2 determined by Hall measurement

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Abstract: Although degenerately doped n^+-2D materials are highly required as sources in 2D tunnel field effect transistor (TFET), the carrier densities for apparent n^+-2D crystals had been qualitatively judged from the negligible gate modulation in I_D-V_G without quantitative analysis so far. Here, the Hall measurement of PtS_2, one of candidate for n^+ source, elucidated that the carrier density is only ~4.1×10^{17} cm^{-3} at 300 K, suggesting that the judgement only from I_D-V_G makes the wrong choice.

1. Introduction

2D TFET is one of promising candidates for devices to achieve not only low power consumption but also high on-current because the band-to-band tunneling (BTBT) results in the subthreshold swing (SS) less than 60 $mVdec^{-1}$ at room temperature (RT) and the tunneling distance can be reduced to the van der Waals distance. Although the complementary operation in TFETs composed of *n*- and *p*-types is required, 2D *p*-TFETs have been limited to few structures in contrast to 2D *n*-TFETs. This problem comes from the lack of air-stable degenerately doped n^+ source 2D crystals. In *p*-TFET, the Fermi level in n^+ source material can be fixed during the gate modulation of channel material, achieving the small SS due to the sharp band alignment switching. Although PtS_2 and $SnSe_2$ are recognized as candidates for n^+ sources based on the qualitative judgement from the negligible gate modulation in I_D-V_G characteristic for thin channel FETs, their carrier densities (n) have never been quantitatively evaluated.

Here, we focus on PtS_2 since it is more suitable than $SnSe_2$ for the source material due to the smaller band gap (E_G) of ~0.25 eV. The thickness dependent I_D-V_G characteristic has been reported on PtS_2 and the negligible V_G modulation of drain current was evident over the channel thickness of ~6 nm.[1] This means that PtS_2 has thinner maximum depletion width (W_{DM}) than ~48-54 nm of MoS_2,[2] typical *n*-type 2D semiconductor. W_{DM} can be estimated from the following relation,

$$W_{DM} = \sqrt{4\varepsilon kT\ln(n/n_i)/q^2 n} \ ,$$

where ε and n_i are dielectric constant and intrinsic carrier density of channel material, respectively. The small W_{DM} of PtS_2 roughly suggests the high doping level, so that PtS_2 becomes the suitable candidate of n^+-source materials. However, according to our I_D-V_G measurement of PtS_2 FET with the channel thickness of 97 nm, it is clear that the current level decreased with decreasing the temperature, as shown in **Fig. 1**. This behavior is inconsistent with the high doping level. In this study, we determined the carrier density of bulk PtS_2 by the Hall effect measurement in order to elucidate the actual carrier density.

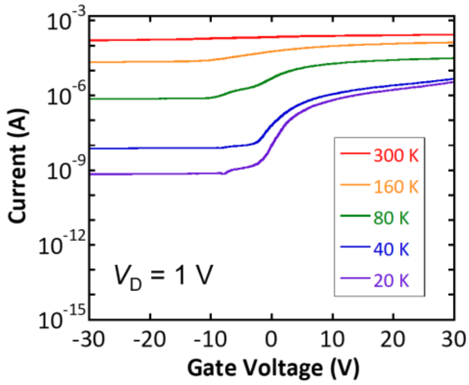

Figure 1. Temperature dependence of I_D-V_G characteristic of PtS_2 FET at V_D = 1 V.

2. Experimental

Figure 2 shows optical micrographs of (a) a Hall device of ~330-nm thick PtS_2 on the SiO_2/n^+-Si substrate and (b) the PtS_2 device mounted on a DIP holder. Electrode patterns were drawn by EB lithography, followed by the deposition of Ni/Au electrodes. All electrodes were connected to the DIP holder with Au wires and Ag paste. Then, the DIP holder with PtS_2 device was placed in the Hall system. By applying magnetic field from 0 to 0.90 T in the *z* direction, the longitudinal voltage (V_H) was measured to determine carrier density based on the following equation,

$$\frac{1}{qn} = \frac{tV_H}{BI_x} \ ,$$

where *t* and *B* are the thickness of the channel and the magnetic field, respectively. Note that the additional

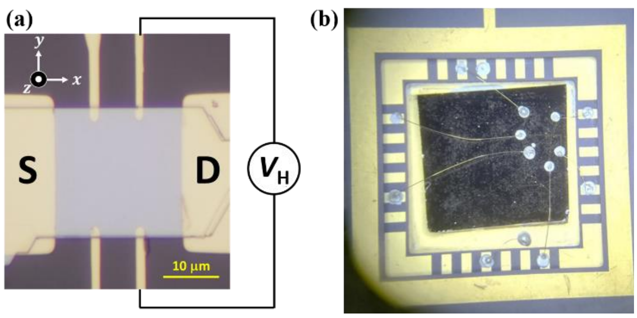

Figure 2. Optical micrographs of (a) PtS_2 Hall device and (b) the DIP holder.

resistance in R_{xy} originated from the miss-alignment between two voltage electrodes was excluded by taking the difference between two sets of R_{xy} obtained under the positive and negative magnetic fields.

3. Hall measurement of bulk PtS_2 FET

As shown in **Fig. 3**, R_{xy} changes linearly with the magnetic field. Hall density is calculated as ~4.1×10^{17} cm^{-3} at 300 K from this slope. Surprisingly, this value is similar level with that of bulk *n*-MoS_2 (~10^{17} cm^{-3}),[3] indicating that PtS_2 is not degenerately doped crystal and the small W_{DM} results from another reason. E_G of PtS_2 dramatically changes from 1.6 eV for monolayer to 0.25 eV for bulk.[1] In short, it can be explained that the reason for small W_{DM} of PtS_2 originates from the large intrinsic carrier density n_i attributed from the small E_G. n_i is indeed calculated as ~2.7×10^{17} cm^{-3}.

In order to get further insights, the temperature dependence of carrier density is measured, as show in **Fig. 4**. The activation energy extracted from the slope is ~2 eV, which is similar to E_G of bulk PtS_2. Therefore, the temperature dependence also supports that small W_{DM} results from small E_G. Although the carriers in typical 2D materials have been generally considered to generate from defects, the intrinsic carriers are dominant due to the small E_G in case of PtS_2.

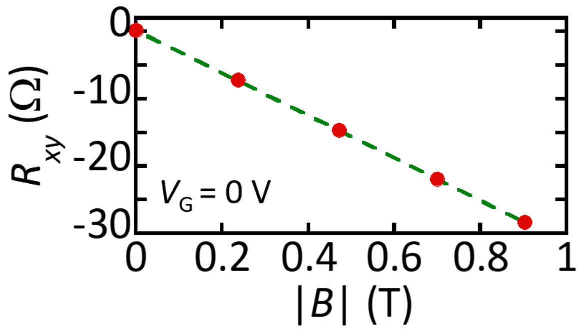

Figure 3. R_{xy} as a function of B at $V_G = 0$ V and 300 K.

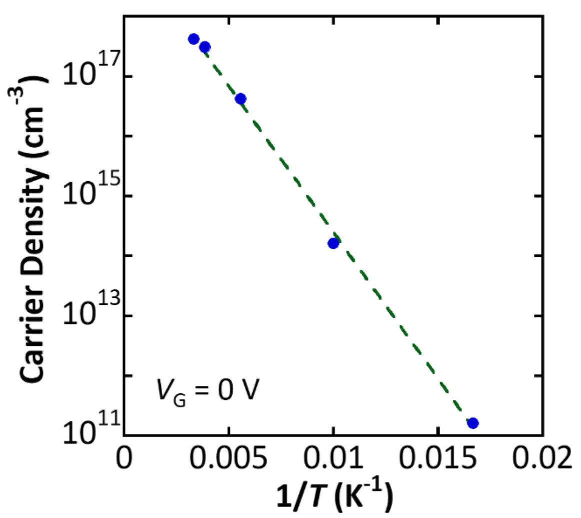

Figure 4. Carrier density as a function of temperatures.

4. Understanding of PtS_2 FET behavior

Based on the carrier density determined by the Hall measurement, the mechanism of temperature dependence of I_D-V_G in **Fig. 1** can be understood as follows. Because n of bulk PtS_2 is only ~4.1×10^{17} cm^{-3}, the bottom surface region of bulk PtS_2 on SiO_2 is modulated by V_G. On the other hand, the upper region of bulk PtS_2 far away from W_{DM} is not affected by V_G due to the screening by the bottom surface region. Taking this into account, two types of mechanisms exist, as shown in **Fig. 5**. In positive V_G range, the current at the bottom surface region becomes dominant because of electron accumulation, while in negative V_G range the residual conductance independent of V_G at the upper region becomes dominant. Although the switching of these two dominant regions is hidden near RT, it becomes prominent when the carrier density is reduced at lower temperatures. Based on this discussion, it is revealed that PtS_2 is not suitable for the source material in TFET due to low carrier density. Even though it apparently shows negligible gate modulation in I_D-V_G at RT, the bottom surface region of bulk PtS_2 modulated to be off-state.

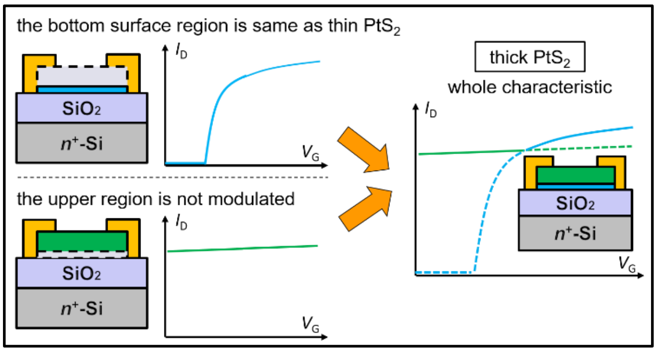

Figure 5. Two dominant current mechanisms in I_D-V_G of bulk PtS_2 FET which is thicker than W_{DM} .

5. Conclusion

The temperature dependent Hall measurement revealed that the carriers of bulk PtS_2 are basically intrinsic and their density is ~4.1×10^{17} cm^{-3} at RT even though bulk PtS_2 FET shows apparent n^+-type I_D-V_G and small W_{DM}. These misapprehensions originate from the residual conductance at the upper region of bulk PtS_2 and considerably small E_G (~0.25 eV) of bulk PtS_2. For selecting the source materials in 2D TFET, the actual carrier density as well as I_D-V_G characteristics at RT should be investigated.

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References: [1] Y. Zhao *et al.*, Adv. Mater. 2016, 12, 2399-2407. [2] N. Fang, *et al.*, ACS Appl. Mater. Interfaces 2018, 38, 32355-32364. [3] M. D. Siao, *et al.*, Nature Commun. 2018, 9, 1442.