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ZrS_2 Ambipolar FETs with Schottky-Barrier Contact to Near-Midgap TiN Film Controlled by Top-Gate TiN/Al_2O_3 Stacks

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Abstract

ZrS_2 ambipolar Schottky barrier (SB) MISFETs are yielded in an operation with both electrons and holes. A layered polycrystalline ZrS_2 thin film was formed by sputtering and sulfur vapor annealing onto a whole surface of 2.4 cm x 2.4 cm SiO_2/Si substrate. A bunch of FETs has a top gate with TiN and Al_2O_3 stacks. Stable ambipolar I-V characteristics are confirmed with a V_{off} value of 0.4 V and an on/off current ratio of 250.

1. Introduction

The scaling of silicon FETs has currently reached down to 5-nm technology node [1,2], however a scaling of energy efficiency has been slowing down, and thus new materials are increasingly required for high-performance FETs. Two-dimensional transition metal dichalcogenide (TMDC) films have unique electrical and physical properties such as a high mobility despite an atomically-thin thickness [3,4,5]. Especially, a zirconium disulfide (ZrS_2) film has a calculated high mobility of more than 1,000 $cm^2V^{-1}s^{-1}$ and band gap of about 1.1 eV. Although the chemical vapor deposition (CVD) method for the synthesis of ZrS_2 film has been reported [6,7], a large area formation has not been reported yet. On the other hand, we have reported that a large-area film formation of layered-polycrystalline ZrS_2 having the high Hall-effect mobility of 1,250 $cm^2V^{-1}s^{-1}$ was remarkably achieved by a sputtering and sulfur annealing [8].

In this study, we demonstrate MISFETs with ZrS_2 thin-film formed by sputtering and sulfur vapor anneal having TiN contacts and a top gate TiN/Al_2O_3 stacks.

2. Device Fabrication

TiN source and drain (S/D) electrodes with 80-nm thickness were formed on a SiO_2/Si substrate by a sputtering and following wet etching. And a ZrS_2 film was formed by an ultra-high-vacuum (UHV) radio frequency (RF) magnetron sputtering tool with a ZrS_2 target of 99% [8]. Then, the sulfur vapor annealing was carried out for sulfur compensation, in which sulfur powder was evaporated at 250ºC for 60 min, and wafers were heated at 700ºC for 60 min in Ar flow under 100 Pa [8]. 20-nm-Al_2O_3 gate insulator was deposited by atomic layer deposition (ALD) at 300ºC with tri-methyl aluminum (TMA) and H_2O precursors, and then an active area was defined by a photolithography and reactive ion etching (RIE). After those, 60-nm-SiN protection was constructed by sputtering and lift-off method, as shown in Figs. 1 and 2. A top gate of TiN film was formed by sputtering and wet etching. Then, S/D contacts through Al_2O_3 gate insulator were fabricated with RIE and sputtering. Finally, a forming gas (F.G.) annealing was conducted at 300ºC for 10 min.

3. Results and Discussion

Fig. 3 indicates I_d-V_{gs} characteristics of ZrS_2 MISFETs with and without F.G. annealing at V_{ds} of 0.05 and 1.0 V. Clear ambipolar transfer characteristics are confirmed in the MISFET at V_{ds} of 1.0 V. The V_{off}, which is extracted at minimum I_d, shifted to a positive side of V_{gs}. This is because positive fixed charges in the Al_2O_3 film are reduced by the F.G. annealing. Fig. 4 shows I_d and I_g-(V_{gs}-V_{off}) characteristics of ZrS_2 MISFETs with and without F.G. annealing. It is speculated that drive-abilities are the same regardless of F.G. annealing. The reduction of the off-current is considered to be due to a termination of an edge of the ZrS_2 channel by hydrogen. From Terada method [9], a parasitic-external resistance (R_{ext}) of 180 GΩ-μm and 2ΔL of -3.0 μm were estimated. Ambipolar g_m characteristics of MISFETs with F.G. annealing are confirmed, as shown in Fig. 5. Because of smaller V_{off} of 0.4 V in this FET, an ambipolar operation of ZrS_2 FETs is explained by the SBFET model [10] in Fig. 6, regardless large electron affinity of 5.71 eV had been reported [5]. According to that, a work function of TiN contact is estimated as near the midgap of ZrS_2 film, and the electrons and holes mainly contribute to I_{ds} in positive and negative V_{gs}, respectively. Fig. 7 shows (I_d, I_s and I_g)-V_{gs} characteristics in which the I_d value directly corresponds to the I_s value in high V_{gs}. In Figs. 8 (a) and (b), saturation characteristics of SBFETs are shown at a range of V_{gs} = 0.5 to -3.0 V for holes and at a range of V_{gs} = 0.5 to 4.0 V for electrons, respectively. The parasitic resistance for holes is larger than that of electrons because the Fermi energy of ZrS_2 channel is upper than the intrinsic energy level.

Table 1 shows a benchmark of ZrS_2 MISFETs with different formation methods. Our FET is superior to other FETs in terms of a small V_{off} of 0.4 V and a high on/off current ratio of ~250, because the contact TiN WF is near a midgap in the bandgap of the sputtered ZrS_2 channel.

4. Conclusions

Chip-level-integrated ambipolar-ZrS_2-SBFETs operating with both holes and electrons were successfully achieved with a smaller V_{off} of 0.4 V for the first time, because of the Fermi level of the ZrS_2 film near the intrinsic energy level and the contact TiN WF near the midgap. This is an important milestone to realize unipolar ZrS_2 n/pFETs.

Acknowledgements

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References

[1] H. Wakabayashi, *et al.*, IEEE Trans. Elec. Devices, (2006), 1961.
[2] G. Yeap, *et al.*, IEDM, (2019), **36**.
[3] D. Lembke, *et al.*, Acc. Chem. Res., **48** (2015), 100.
[4] W. Zhang, *et al.*, *Nano Research*, **7** (2014), 1731.
[5] C. Gong, *et al.*, *Appl. Phys. Lett.*, **107**, (2015), 139904.
[6] M. Zhang, *et al.*, *J. Am. Chem. Soc.*, **137**, (2015), 7051.
[7] X. Wang, *et al.*, *J. Mater. Chem. C*, **4**, (2016), 3143.
[8] M. Hamada, *et al.*, *IEEE JEDS*, **7**, (2019), 1258.
[9] K. Terada, *Elect. Comm. JPN*, **79**, (1996), 43.
[10] F. Wang, *et al.*, *Adv. Mat.*, **31**, (2019), 1805317.

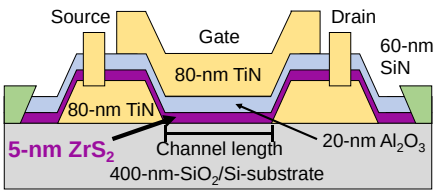

Fig. 1 Cross-sectional schematic diagram of ZrS_2 MISFET.

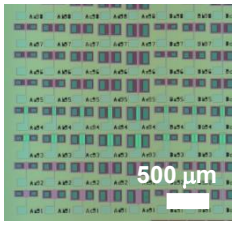

Fig. 2 Optical image of MISFET array whose channel length and width are varied.

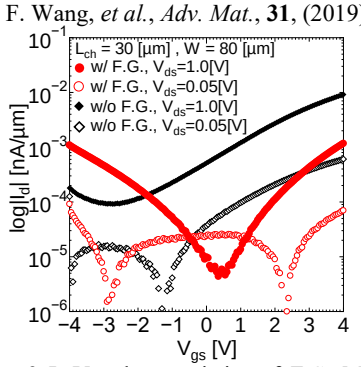

Fig. 3 I_d-V_{gs} characteristics of ZrS_2 MISFET w/ and w/o F.G. annealing for L_{ch} of 30 μm and W of 80 μm at V_{ds} of 1.0 V. V_{off} is extracted at minimum I_d.

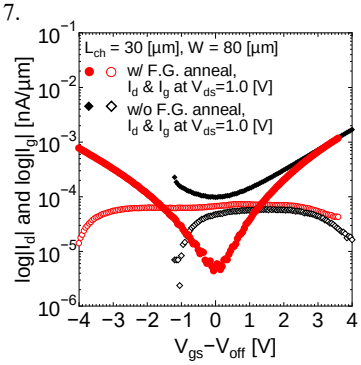

Fig. 4 I_d and I_g-(V_{gs}-V_{off}) characteristics of ZrS_2 MISFET w/ F.G. annealing for L_{ch} of 30 μm and W of 80 μm at V_{ds} of 1.0 V.

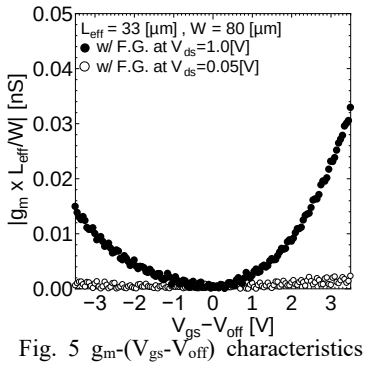

Fig. 5 g_m-(V_{gs}-V_{off}) characteristics of ZrS_2 MISFET w/ F.G. annealing for L_{eff} of 33 μm and W of 80 μm at V_{ds} of 1.0 V.

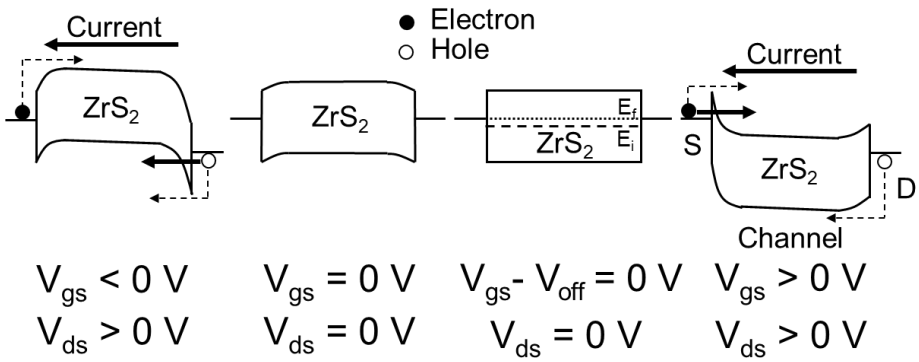

Fig. 6 Band diagrams under different gate voltage ranges with the Schottky-barrier FET model using ZrS_2 FET. The close and open circles indicate electrons and holes, respectively.

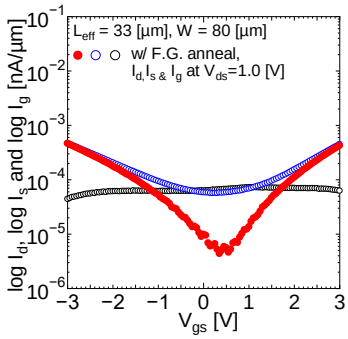

Fig. 7 I_d, I_s, & I_g -V_{gs} characteristics of ZrS_2 MISFET w/ F.G. annealing for L_{ch} of 30 μm and W of 80 μm at V_{ds} of 1.0 V.

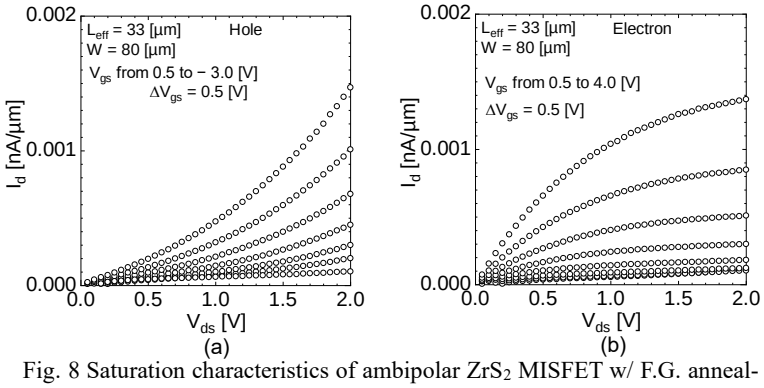

Fig. 8 Saturation characteristics of ambipolar ZrS_2 MISFET w/ F.G. annealing for L_{eff} of 33 μm and W of 80 μm, operating with (a) hole and (b) electron.

Table 1: Benchmark of reported ZrS_2 FETs with different film formation methods.

Method	Sputter this work	CVD [3]	CVD [4]
Precursors	ZrS_2 & sulfur	$ZrCl_2$ & sulfur	$ZrCl_2$ & sulfur
Temp. [°C]	**700**	760~	950
Thick. [nm]	~5.0	0.71	a few-layers
Gate	**Top**	Bottom	Bottom
Operation	**Ambipolar**	Unipolar (e)	Unipolar (e)
V_{off} [V]	**0.4 (e/h both)**	- 40	- 10
On/off	**~ 250**	~ 15	~ 25
Mobility [$cm^2V^{-1}s^{-1}$]	e: ~ 0.0001 h: ~ 0.0001	0.1-0.8	~ 0.1