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ALD-ZrO_2 Gate Dielectric with Suppressed Interfacial Oxidation for High Performance MoS_2 Top Gate MOSFETs

Wen Hsin Chang[1], Naoya Okada[1], Masayo Horikawa[1],
Takahiko Endo[2], Yasumitsu Miyata[2] and Toshifumi Irisawa[1]
[1] National Institute of Advanced Industrial Science and Technology (AIST), Japan
[2] Department of Physics, Tokyo Metropolitan University, Japan
Email: wh-chang@aist.go.jp

Abstract **—To enhance the feasibility of 2D transition metal dichalcogenide channels in nano-electronic devices, a top gate device structure fabricated with Very-Large-Scale-Integration compatible process is desired. High-κ dielectric ZrO_2 has been directly deposited on MoS_2 through low temperature atomic layer deposition. Physical adsorption instead of chemical reaction was confirmed at the interface between ZrO_2 and MoS_2, which helps to suppress interfacial oxidation and reduce damage. While scaling down capacitance equivalent thickness of ZrO_2, low thermal budget post deposition annealing was effective for reducing interfacial traps, thus enhancing the device performances of monolayer MoS_2 nMOSFETs.**

1. Introduction

Atomic-layer transition metal dichalcogenides (TMDCs) have attracted considerable attention owing to their promising properties for future nano-electronic applications. MoS_2, a well-known TMDC channel material shows great potential in low-power-consumption device field. To fulfill the requirement of VLSI (Very-Large-Scale-Integration) applications, fabricating high performance top gate MoS_2 MOSFETs using chemical vapor deposition (CVD) grown MoS_2 with high quality gate dielectric is indispensable. However, because of the lack of surface dangling bonds, it is still very challenging to obtain high quality high-κ/MoS_2 interface with low capacitance equivalent thickness (CET) through atomic layer deposition (ALD) approach [1,2]. Recently, we have reported uniform deposition of ZrO_2 on CVD-grown MoS_2 by plasma enhanced ALD (PEALD) [3], which showed the decent device performance and high dielectric constant. Although high oxidation efficiency of PEALD promotes uniform layer deposition, the degradation of interfacial quality owing to MoS_2 oxidation was addressed. In order to further enhance device performance as well as gate control of channel, optimization of ALD processes not to damage the surface of 2D materials and CET scaling of ZrO_2 are necessary.

In this work, uniform deposition of ZrO_2 as gate dielectrics on CVD-grown MoS_2 were obtained through ALD even at low deposition temperature at 150 °C, leading to significantly suppressed interfacial oxidation. The CET scaling of ZrO_2 down to 2.3 nm was also demonstrated. In addition, the top gate monolayer (1L) MoS_2 MOSFETs exhibited reduced subthreshold swing (SS) and improved hysteresis as the benefits of low temperature post deposition annealing (PDA) and CET scaling.

2. Experimental

The detailed process flow for fabricating 1L MoS_2 top gate MOSFETs is shown Fig 1(a). The schematic cross-section and top view of optical microscope photograph of MoS_2 devices are shown in Fig. 1(b) and 1(c), respectively. Salt-assisted CVD was used to synthesize MoS_2 directly on SiO_2 (285 nm)/Si substrates using MoO_2 and sulfur powder. KBr was used as a growth promoter, as described previously [4]. After 1L MoS_2 growth, the S/D contacts were formed with photolithography and e-beam evaporation. Then, the ZrO_2 gate dielectrics were deposited at 150 °C thorough ALD using TEMAZ and H_2O as precursors with different deposition cycles, which denotes as LT-ALD afterwards. Finally, after 300 °C PDA in N_2 ambient, the top gate electrodes were deposited through e-beam evaporation. Top gate MoS_2 MOSFETs with PEALD ZrO_2 gate dielectrics deposited at 300 °C [3] were also prepared for comparison, which denotes as HT-PEALD afterwards.

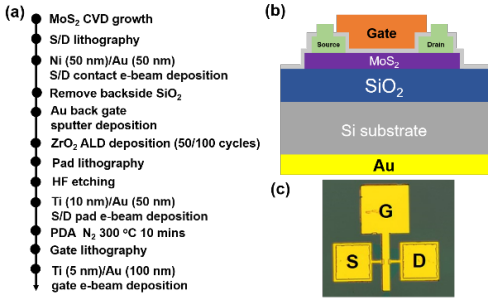

Fig. 1(a) Process flow for fabricating MoS_2 top gate MOSFETs, (b) schematic cross-section and (c) top view of optical microscope photograph of the fabricated devices.

3. Results and Discussion

Fig. 2 shows the HR-TEM cross-sectional image of MoS_2 channel with LT-ALD ZrO_2 gate dielectric. The channel thickness of 0.7 nm, corresponding to 1L MoS_2, is clearly seen with the abrupt ZrO_2/MoS_2 interface.

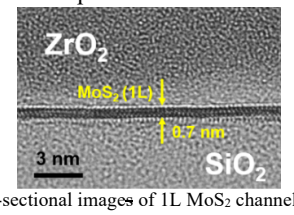

Fig. 2 HR-TEM cross-sectional images of 1L MoS_2 channel with ALD-ZrO_2 gate dielectric.

Fig. 3(a) shows Mo 3d XPS spectra extracted from 2-nm-thick ZrO_2 on bulk MoS_2, which was mechanically exfoliated from MoS_2 flakes. The spectrum extracted from pristine MoS_2 flakes was also shown for comparison. The Mo 3d spectra for pristine and LT-ALD samples show similar feature with three peaks, which are attributed to the doublet of Mo^{4+} $3d_{3/2}$ and Mo^{4+} $3d_{5/2}$ and S^{2-} 2s states in MoS_2. This

indicates the ZrO_2 deposition at 150 °C mainly results from physical absorption instead of chemical reaction between ZrO_2 and MoS_2. On the other hand, additional Mo^{6+} $3d_{3/2}$ and Mo^{6+} $3d_{5/2}$ states, correlating to MoO_3 were observed in HT-PEALD samples. This suggests the existence of Mo oxide interfacial layer owing to high oxidation efficiency of high temperature PEALD, which also explain the difficulty in obtaining device operation of 1L MoS_2 devices with PEALD ZrO_2 gate dielectrics [3]. Meanwhile, no obvious difference was observed in S 2p XPS spectra as shown in Fig. 3(b), which exhibited two peaks resulting from the doublet of S^{2-} $2p_{1/2}$ and S^{2-} $2p_{3/2}$ states in MoS_2. All these peaks are consistent with the reported values for MoS_2 crystal.

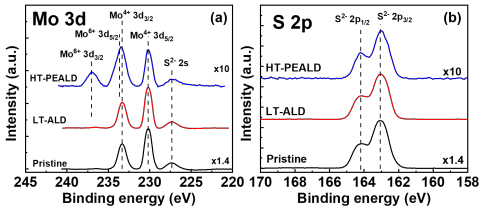

Fig. 3(a) Mo 3d and (b) S 2p XPS spectra extracted from HT-PEALD ZrO_2/MoS_2, LT-ALD ZrO_2/MoS_2 and pristine MoS_2, respectively.

The impact of ZrO_2 deposition on the device performance of MoS_2/SiO_2 back gate transistors was investigated. Fig. 4 shows the I_D-V_G transfer curves extracted from MoS_2 MOSFETs under back gate operation before and after ZrO_2 deposition on top of the MoS_2 surface. Even with 2-layer (2L) MoS_2 channel, those devices with HT-PEALD ZrO_2 demonstrate degraded features in terms of lower on-state current and worse SS after ZrO_2 deposition. On the other hand, no obvious degradation was found in LT-ALD 1L MoS_2 case, indicating the benefits of low temperature ALD process to suppress damages due to oxidation of MoS_2 surface. Less damage of MoS_2 channel with no interfacial layer is consistent with the result in Fig. 2.

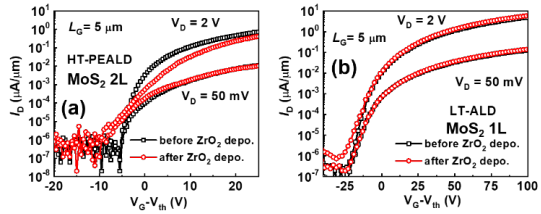

Fig. 4 I_D-V_G transfer curves extracted from MoS_2 MOSFETs under back gate operation before and after (a) HT-PEALD and (b) LT-ALD ZrO_2 encapsulation on top of MoS_2 surface.

To understand the influence of low thermal budget PDA, Fig. 5 (a) shows the I_D-V_G characteristics of 5 μm-gate-length 1L MoS_2 MOSFETs under top gate operation measured before and after 300 °C PDA. Normal nMOSFETs operation behaviour was clearly observed with a high on-off ratio of 10^7 after PDA. It was found the low thermal budget PDA is effective for reducing interfacial traps, since the SS drastically decrease from ~170 to ~90 mV/decade after PDA as shown in Fig. 5(b). As the scattering factor suppressed, enhanced on-state current was also obtained. (Fig. 5(a)) Besides, the drain induced barrier lowering (DIBL) was also significantly reduced, which may be attributed to the improvement of contact resistance after PDA.

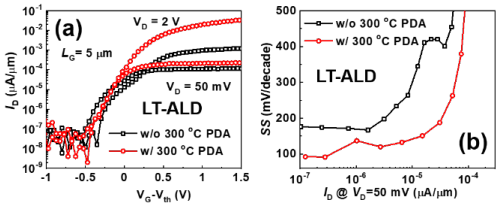

Fig. 5 (a) I_D-V_G characteristics of 5 μm-gate-length 1L MoS_2 top gate MOSFETs measured before and after 300 °C PDA and (b) The I_D dependence of extracted SS.

The CET scaling effect on device performance was also characterized. Fig. 6(a) shows the split-CV curves at frequency of 10 kHz extracted from MoS_2 nMOSFETs with ZrO_2 deposited with ALD 50 and 100 cycles. Based on maximum C_{ox}, the CET was determined to be 2.3 and 4.4 nm. The dielectric constant of ZrO_2 was calculated to be 13.4 by using ZrO_2 physical thickness, which was relatively lower than that of HT-PEALD samples [3]. The deposition temperature induced phase transition may explain this phenomenon, and this can be avoided by optimizing ALD conditions and/or PDA. Fig. 6(b) shows gate hysteresis curves for 1L MoS_2 devices with different CET. Decent device performance maintained with CET shrinking down to 2.3 nm. Higher on-state current with reduced gate hysteresis, indicating the benefits of CET scaling.

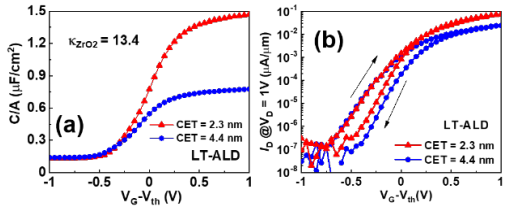

Fig. 6(a) Split-CV characteristics at frequency of 10 kHz and (b) I_D-V_G hysteresis curves at V_D of 1 V extracted from 1L MoS_2 devices with different ALD growth cycles.

4. Conclusion

1L MoS_2 top gate MOSFETs using ALD ZrO_2 gate dielectrics has been demonstrated with VLSI-compatible gate stack formation processes. Low ALD deposition temperature promotes physical adsorption, leading to significantly suppressed surface oxidation and less damaged MoS_2 channel. Decent operation behavior maintained while ZrO_2 CET scaling down to 2.3 nm, indicating the low thermal budget process is beneficial for MoS_2 channel. Further CET scaling would be expected by ZrO_2 thickness scaling.

Acknowledgements

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Reference

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