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Understanding the tunneling behavior in 2D based floating gate type memory device by measuring floating gate voltage

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Abstract: In this study, tunneling behavior in 2D based floating gate (FG) type memory devices was studied. Although three kinds of memory devices with different channel materials ($MoTe_2$, WSe_2 and MoS_2) showed the similar memory window in I_d-V_G sweep, FG voltage measurement proposed here exhibited the three different potential trajectories. The detailed analysis on tunneling behavior elucidated that these difference resulted from the properties of the generation of electron-hole pair in channel and metal/2D contact as well as main tunneling path of *h*-BN.

1. Introduction

2D materials based floating gate (FG) type memory devices have been widely studied as a candidate of next generation non-volatile memory device [1-3]. Although its operation was usually demonstrated by I_d-V_G double sweep curve with large memory window, the details of tunneling behavior between FG and channel during I_d-V_G sweep is still unclear. Moreover, how the tunneling behavior depends on channel materials is also unclear while there are many candidates for 2D semiconductor channel. This prevents us to design channel material appropriately and to discuss about its performances such as retention and endurance.

In this study, floating gate voltage (V_{FG}) measurement was proposed to understand the tunneling behavior in 2D based FG type memory device. From the results, capacitive coupling region and tunneling region can be distinguished and its difference was clearly observed in each device which I_d-V_G curves cannot clarified. Since not only *h*-BN but also channel and metal/2D contact should be considered as the tunneling current path to guarantee the tunneling within 2D hetero-stack, three kinds of tunneling behavior was clearly distinguished depending on current limiting path. The analysis on each tunneling behavior clarified the difference of each device resulted from the properties of channel materials.

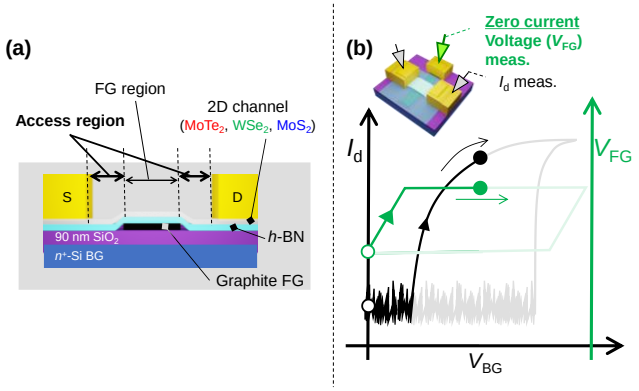

Fig. 1 (a) Cross sectional view of fabricated memory devices and (b) schematics of V_{FG} measurement condition. V_{FG} was measured in zero current condition. I_d and V_{FG} ware measured simultaneously.

2. Results and Discussion

The cross sectional view of fabricated memory devices is illustrated in **Fig. 1 (a).** While three kinds of devices with different channel materials were fabricated in this study, the device structure and fabrication procedure are the same. Mechanically exfoliated 2D materials were sequentially stacked on 90 nm SiO_2/n^+-Si substrate. 2D semiconductor ($MoTe_2$, WSe_2 or MoS_2) was used as a channel, *h*-BN and graphite were used as a tunneling barrier and FG, respectively. Ni/Au were thermally deposited as metal electrodes. Noted that the access region (channel region not overlapped with FG) was secured to guarantee the tunneling within 2D hetero-stack. The channel over the FG is called FG region in this paper.

V_{FG} measurement condition is schematically shown in **Fig. 1 (b)**. Additional electrode was attached to FG for measuring its potential. V_{FG} as well as I_d was measured with zero current condition during V_{BG} sweep.

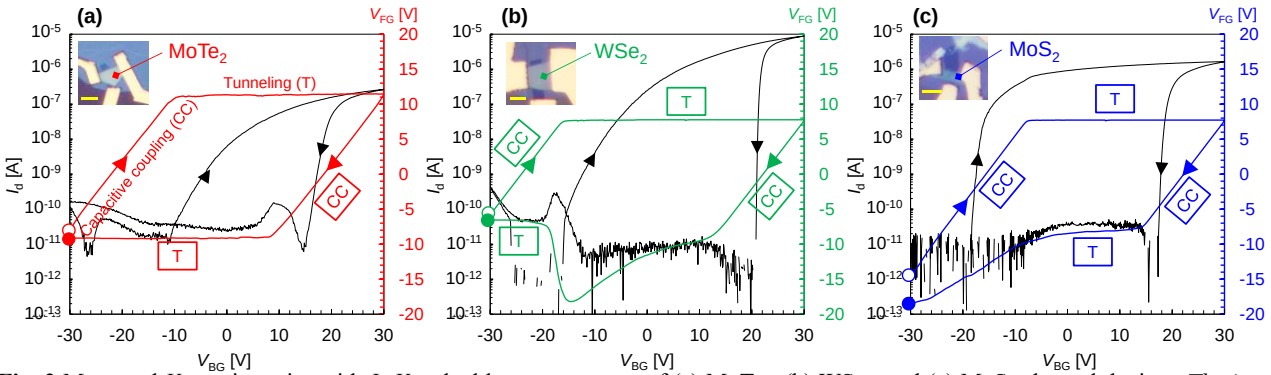

Fig. 2 Measured V_{FG} trajectories with I_d-V_{BG} double sweep curves of (a) $MoTe_2$, (b) WSe_2, and (c) MoS_2 channel devices. The inset shows the optical images of fabricated devices. Open and filled circle symbols indicate start and end points of V_{FG} trajectory, respectively. The capacitive coupling region (CC) and tunneling region (T) can be distinguished for each device. The shape of V_{FG} trajectories strongly depends on channel materials. All measurements were conducted at room temperature. Scale bar represents 5 μm.

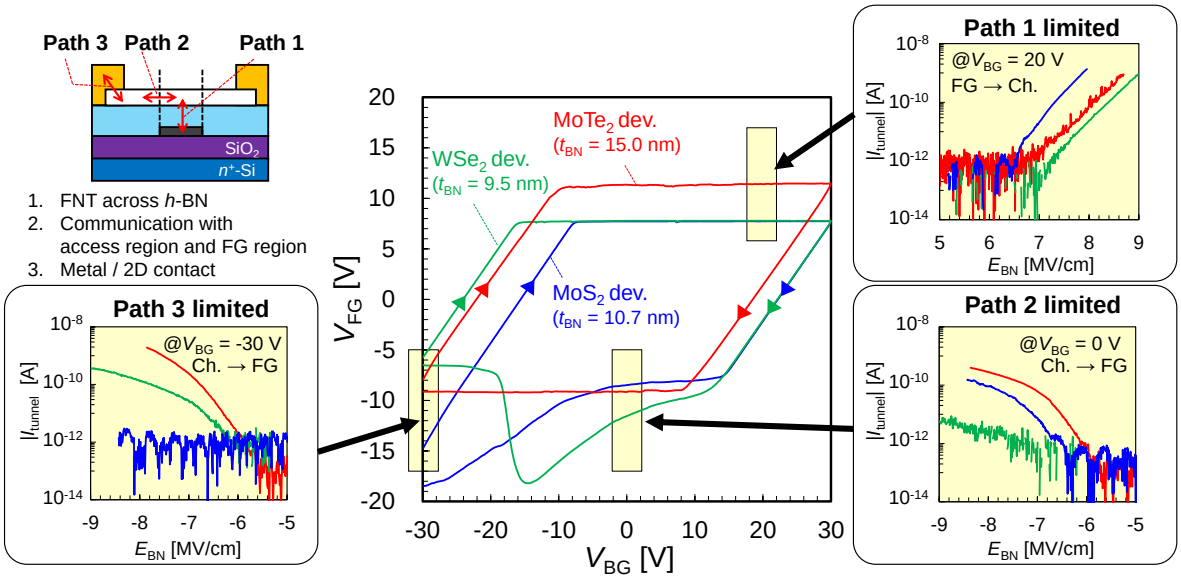

Fig. 3 The summary of tunneling conditions during I_d-V_{BG} double sweep based on V_{FG} trajectories. In this device structure, three tunneling paths should be considered as shown in upper left. Three distinct tunneling behavior (I_{tunnel} as a function of E_{BN}) are shown. Path 1 limited tunneling (FN tunneling across *h*-BN, V_{BG} = 20 V, V_{FG} > 0 V), path 2 limited tunneling (generation at *pn* junction in the channel, V_{BG} = 0 V, V_{FG} < 0 V) and path 3 limited tunneling (hole injection from Ni electrode, V_{BG} = -30 V, V_{FG} < 0 V).

Measured V_{FG} trajectories with I_d-V_{BG} of three different channels are compared in **Fig. 2**. These V_{FG} trajectories can be understood as follows. 1) Linear and steep increase/decrease in V_{FG} result from capacitive coupling with back gate (BG). 2) Flat V_{FG} indicates that tunneling occurred here. Although capacitive coupling also occurred here, charged carrier tunneling took the FG potential (V_{FG}) back to the potential at which tunneling started. Therefore, non-linear or gradual change of V_{FG} suggests that tunneling current was not large enough to take V_{FG} back to the tunnel start voltage.

For further discussions, tunneling current between channel and FG was measured with grounded source by sweeping V_{FG}, where V_{BG} was fixed at the constant value. In this device structure, there are no substrate terminal in contrast to Si-based FG-type memory device and access region guarantee that the tunneling occurs within the 2D hetero-stack. Therefore, as shown in upper left of **Fig. 3**, not only the *h*-BN insulator (path 1) but also the channel between access region and FG region (path 2) and metal/2D contact (path 3) should be considered as the tunneling current path. Therefore, three distinct tunneling behavior was observed, depending on which path limits the current flow between FG and source electrode, as shown in **Fig. 3**. Measured tunneling current was plotted as a function of E_{BN} that is electrical field across *h*-BN. The E_{BN} was calculated by V_{FG}/t_{BN}, where t_{BN} is the thickness of *h*-BN measured by AFM.

At first, upper right of **Fig. 3** shows path 1 limited tunneling at V_{BG} = 20 V with positive E_{BN} (tunneling current from FG to channel). Since both V_{BG} and V_{FG} is positively large enough in this region, channel polarity of both FG region and access region is *n*-type since FG can be considered as the local BG. It means that electron is easily injected from Ni to the channel and there are no *pn* junctions at the path 2. Therefore, path 1 should be a limiting path. In addition, the linear relationship in FN plot has been confirmed for each device. Next, Path 2 limited tunneling at V_{BG} = 0 V with negative E_{BN} (tunneling current from channel to FG) is shown in lower right of **Fig. 3**. In this region, V_{BG} is positive while V_{FG} is negative due to capacitive coupling with BG whose voltage (V_{BG}) was swept from 30 V to negative direction. It means that FG region is *p*-type and access region is *n*-type. Although *pn* junction was formed at the path 2, the tunneling current flows from source to FG, that is, from *n*-type access region to *p*-type FG region. This may be attributed to the generation of electron-hole pair at *pn* junction at the path 2. It was confirmed that these tunneling current was decreased with decreasing temperature and finally vanished. Linear relationship was not observed in the FN plot. Finally, path 3 limited tunneling at V_{BG} = -30 V with negative E_{BN} (tunneling from channel to FG) is shown in lower left of **Fig. 3**. In this region, both FG and access regions are *p*-type since both V_{BG} and V_{FG} is negatively large enough. However, it is well known that, MoS_2 shows only *n*-type conduction due to strong Fermi level pinning at the metal/MoS_2 contact [4] while WSe_2 and $MoTe_2$ have ambipolar nature [5,6]. Therefore, tunneling current was limited by hole injection from Ni and it cannot be observed only for MoS_2 device even though E_{BN} is high enough and no *pn* junction was formed at the path 2. In this way, the details of tunneling behavior can be understood.

3. Conclusion

The difference of tunneling behavior in each channel material based memory device can be understood by employing proposed V_{FG} measurement. V_{FG} measurement is strongly suggested to be powerful tool to understand the tunneling behavior in 2D based FG type memory devices. Moreover, since V_{FG} can be easily measured in other configurations of memory devices, this knowledge will enable us to discuss the details of memory operation and its performances.

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